BARADWAJ VIGRAHAM

CONTACT INFORMATION

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INTERESTS

Analog/Mixed signal/RF Integrated circuit design

EDUCATION

Columbia University, New York *August 2008 - Present*

- Doctoral track program (M.S-Ph.D) in Analog/RF IC design
- Grade Point Average: **4.05**/4.00 (as of Spring 2010)
- Master of Science (M.S) degree awarded in February 2010

Indian Institute of Technology Madras (IIT Madras), Chennai, India *August 2004 - April 2008*

- Bachelor of Technology (B.Tech) in Electrical Engineering
- Minor in Physics
- Cumulative Grade Point Average: **9.23**/10

ACADEMIC ACHIEVEMENTS

- Was ranked **206** out of over 150,000 candidates in Joint Entrance Examination (JEE) for Indian Institutes of Technology *2004*
- Was ranked **38** out of over 500,000 candidates in All India Engineering Entrance Exam (AIEEE) *2004*
- Was awarded the Pratibha merit award by the Government of Andhra Pradesh, India *2004*
- Was awarded the Armstrong Memorial Award for M.S students by the Electrical Engineering department at Columbia University for outstanding performance *2009-2010*
- Was awarded the Analog Devices Outstanding Designer Award by Analog Devices Inc. *2012-2013*

TEACHING

- Teaching assistant for Introduction to Electrical Engineering *Fall '08*
- Teaching assistant for Advanced Analog Integrated Circuits *Spring '09*
  - Involved in designing a basic set of assignments and examinations
  - Helping with designing a more extensive set of assignments and project *Spring '12*

PUBLICATIONS *(chronologically)*

- **B. Vigraham**, P. Kinget, "A Self-Duty-Cycled and Synchronized UWB Receiver SoC Consuming 375pJ/b for -76.5dBm Sensitivity at 2Mbps," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2013
- V. Singh, N. Krishnapura, S. Pavan, **B. Vigraham**, D. Behera, N. Nigania, "A 16MHz BW 75dB DR CT $\Delta\Sigma$ ADC compensated for more than one cycle excess loop delay," IEEE Journal of Solid State Circuits (JSSC), Aug. 2012
- **B. Vigraham**, P. Kinget, "An Ultra Low Power, Compact UWB Receiver with Automatic Threshold Recovery in 65 nm CMOS," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Jun. 2012
- G. Stanje, P. Miller, J. Zhu, A. Smith, O. Winn, R. Margolies, M. Gorlatova, J. Sarik, M. Szczodrak, **B. Vigraham**, L. Carloni, P. Kinget, I. Kymissis, and G. Zussman, Demo: Organic solar cell-equipped energy harvesting active networked tag (EnHANT) prototypes, in Proc. ACM SenSys11, Nov. 2011
  - Received the best student demo award

- V. Singh, N. Krishnapura, S. Pavan, **B. Vigraham**, N. Nigania, D. Behera, "A 16MHz BW 75dB DR CT $\Delta\Sigma$ ADC compensated for more than one cycle excess loop delay," IEEE Custom Integrated Circuits Conference, Sep. 2011
- J. Zhu, G. Stanje, R. Margolies, M. Gorlatova, J. Sarik, Z. Noorbhaiwala, P. Miller, M. Szczodrak, **B. Vigraham**, L. Carloni, P. Kinget, I. Kymissis, and G. Zussman, "Demo: Prototyping UWB-Enabled EnHANTs", Proc. ACM MobiSys'11, Washington, DC, Jun. 2011

RESEARCH EXPERIENCE

- **Ultra low power UWB transceiver design** *Ph D thesis*
  There has been an increased interest in the area of Impulse Radio UWB (IR-UWB) transceivers targetted at very low data rate applications (<10-20 Mbps). Communication is achieved by means short ($<$ 4 ns) RF pulses of energy repeating at a rate comparable to the desired data rate. This allows for transceiver power down during communication silence for reduced energy consumption. Neigbouring narrowband technologies like Wimax (802.16) and Wifi (802.11) present significant challenges in the design of UWB radios tolerant to interference. Additional challenges include achieving sharp dutycycling of the receivers to lower their power consumption and synchronization between the transmit and receive nodes to achieve the same. This calls for a cross layer design and optimization of circuits and systems including complete transceivers and low power frequency references and forms the primary focus of this thesis.
- **Low area phase shifters** *Internship at Kilby Labs, Texas Instruments, Dalls, Summer '11*
  Developed a low area passive phase shifter for millimeter wave radio.
- **High linearity RF frontends for TV tuners** *Internship at Silicon Laboratories, Austin, Summer '10*
  An investigative attempt was made to integrate active splitters with existing TV tuners for Picture-in-Picture applications. The primary challenge lies in the design of a highly linear ($\geq$ 25 dBm IIP3) LNA in Silicon on a 2.7 V supply. A novel, highly process tolerant distortion cancelling technique was proposed for this purpose. Relying on and limited only by matching between CMOS transistors, this technique can be used to circumvent the distortion of the common source stage in Noise cancelling LNAs.
- **Analog IC design tradeoffs with CMOS scaling** *Internship at Silicon Laboratories, Austin, Summer '09*
  A comparison of 130nm and 65nm CMOS technologies for various analog design tradeoffs was performed. A PLL was used as a test structure for comparison
- **Sub nano-second flash ADC for 800 Msps CT $\Delta\Sigma$ modulator** *Undergraduate thesis*
  A Flash ADC was designed to be clocked at 1 GHz for use in a continuous time $\Delta\Sigma$ modulator was designed and verified for performance on a 0.18 μm UMC process. It has a delay of 300-400ps depending on the input it samples. The flash output is passed through a source follower to level shift the output common mode and to improve driving capability. The output of the source followers was fed to a differential pair terminated with ideal resistors and the time elapsed between the sampling clocks sampling instant and the switching time of the output of the differential pair was used to measure the above mentioned delay. It produces a in-band SNR of 97.1dB with ideal blocks for the loop filter and the DAC in the $\Delta\Sigma$ modulator.
- **Analysis of Feedback Systems** *An Internship at Texas Instruments India, Chennai, Summer '07*
  The internship was aimed at finding the best method to predict or estimate the stability of a feedback system without the knowledge of subjective details like the type of feedback. In other words, the stability had to be predicted from terminal characteristics. Several techniques proposed in the literature like cutting the loop to estimate the return ratio, Voltage and current injection and Null double injection proposed by Middlebrook, etc. were analysed and weighed. It was found that cutting the loop at any point disturbs the existing system and the return ratio so estimated will be erroneous. It was finally concluded that the best method would be to estimate the loop gain from the two-port parameters of the system. These results were then applied to explain the instability of an LDO (Low Drop Out Regulator) and it was concluded the two-port approach works only if there is prior knowledge of the common mode rejection of the differential amplifiers in the circuit. In the case that the common mode propogates in the circuit, the system is best modelled as a 3-port to estimate the loop gain.

RELEVANT COURSEWORK

Active filter design
VLSI Data Conversion circuits

VLSI Broadband communication circuits
at IIT Madras

Advanced Communication circuits
Analog systems in VLSI
Digital Communication
Circuit theory
Seminar (Power amplifiers)

MOS Transistors
Microwave circuits
Seminar (RF and millimeter wave design)
Wireless and Mobile communication I
at Columbia University