E6312 Homework 2
Due 13th Feb 2009

February 9, 2009

1 Problem 1

For a nMOS transistor of size $\frac{1\mu}{0.18\mu}$ biased at $V_{GS} = 0.8$ V and $V_{BS} = 0$ V, plot C_{gs}, C_{gd}, C_{bd} as a function of V_{DS}. Use AC analysis with a thoughtfully selected test circuit to perform the measurements, and compare them with those obtained from DC operating point simulations.

Here is a how to do for AC Simulation: `http://www.columbia.edu/~yf2162/acSiml.html` by Anuranjan Jha. You can also consult the tutorial from the previous assignment. Remember the capacitance is the ratio between charge an voltage, or alternatively the current through a capacitor is related to voltage by frequency and capacitance, $V_C = \frac{I_C}{2\pi f C}$

2 Problem 2

In this problem, we investigate the most common biasing schemes used in IC design. Unlike discrete component design, in IC design we often do not AC couple stages unless otherwise necessary and hence proper design of bias circuits is essential. Consider the biasing of a differential pair shown in figure 1. All device sizes are indicated in the figure. The differential pair is intended to be operated with all transistors in saturation in strong inversion. In other words, assume that the inputs to the differential pair are small and swing around some bias voltage v_{bias2}(or equivalently the current through the two transistors M2, M3 is approximately $\frac{I_{tail}}{2}$).

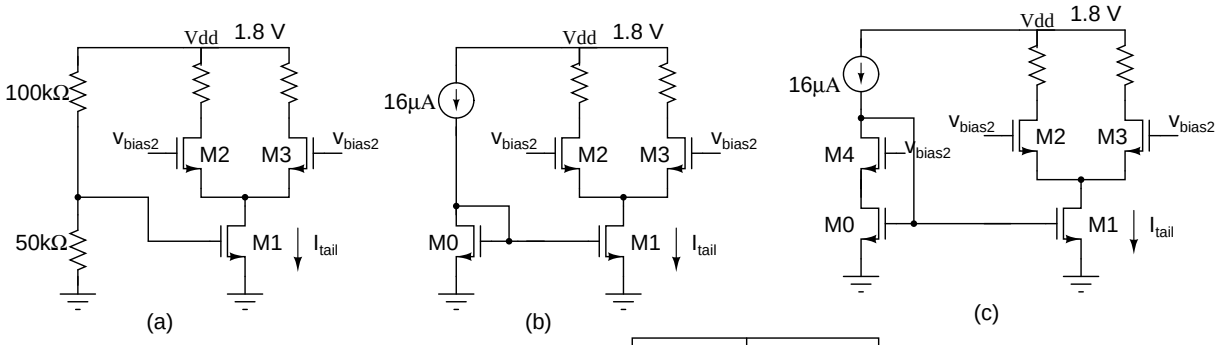
1. Assuming a square law model with $\beta = 320\frac{\mu A}{V^2}$ where $I_{DS} = \frac{\beta}{2}\frac{W}{L}(V_{GS} - V_{th})^2$ and a $V_{th} = 500$ mV, calculate the tail current I_{tail} marked in the circuit. Calculate the g_m of the transistors M2, M3.

2. Due to various imperfections in IC fabrication, temperature variations and other reasons, the parameters β, V_{th} etc., change from one chip to another. These are termed process corner and temperature variations. A slow corner is one in which V_{th} is higher than normal and a fast corner is one in which V_{th} is lower than normal. Suppose due to process corner variations, V_{th} changes to 550 mV. Calculate I_{tail} and g_m of M2, M3 now. What do you observe? This is the reason why biasing with an absolute voltage is often avoided in IC design.

3. Now consider the biasing scheme described in figure 1(b). Here the gate voltage applied to the transistor M1 is obtained by biasing a similar transistor (M0) using a reference current source. If we assume all transistors have infinite output impedance, what is the current I_{tail}? If instead the transistors M0 and M1 have a $g_m r_o$ of 10, and the drain of M1 is assumed to be at 550 mV, what is the value of I_{tail} ? (Hint: use small signal analysis to provide a rough estimate of the current)

4. Assuming square law, what is the minimum bias voltage (in terms of v_{th} and I_{ref}) required for the gates of M2 and M3? How will you generate this voltage without any additional current source? How sensitive is the circuit to this voltage?

5. Consider the biasing scheme in figure 1(c). Do you think the current mirrored in to the transistor M1 would be exactly the same as that pushed in to M0? Why? Here we try to further improvise the current mirrored in to M1. What do you think is the reason behind a claim that this scheme is better than the scheme shown in figure 1(b). For best results, what should the size of the device M4?



M0, M1	2.5μ/0.25μ
M2, M3	1.25μ/0.25μ

Figure 1: Biasing schemes

6. Extra credit: If instead of opearting the transistors M2 and M3 such that both of them are in saturation and strong inversion, we operate such that the current is always present in either M2 or M3. In other words, at any point of time, one of M2 and M3 carries I_{tail} and the other will carry 0. Then what would be the best choice for the size of the device M4?

3 Problem 3

Consider the following "synthesis" of a source follower(VCVS) from elementary circuit theory using feedback:

We wish to make incremental voltage of v_{out} equal to that of v_{in} to build a voltage controlled voltage source (VCVS). We restrict ourselves to the use of a voltage controlled current source (VCCS) of infinite transconductance (g_m) as the error amplifier in feedback (because that is the best model for a transistor). In the figure 2(a) is shown the starting point where we compare the input and output voltage and a current which is proportional to the error is produced in the current source. The feedback block X has to correct v_{out} such that there is no excitation from the error amplifier. In other words, when the error amplifier sees that $v_{in} > v_{out}$, v_x increases and this should translate to increasing v_{out} and when the error amplifier sees that $v_{in} < v_{out}$, v_x decreases and this should translate to the v_{out} going down. One way of implementing the block X would then be to connect v_x to v_{out} (since there is no inversion of sign. If an inversion of sign were required, we would not have been able to do this). This is shown in figure 2(c) and this is the small signal equivalent circuit of the well known source follower shown in figure 2(d).

Another method is shown in figure 2(b) where we can put an amplifier between v_x and v_{out}. However, if this has to be translated in to a transistor, the node v_x has to be connected to v_{out}. The only way to sense the error signal would be to sense the other end of the current source and provide feedback to v_{out}. This is shown in figure 2(e) and this leads to what is shown in figure 2(f). The topologies derived from 2(f) are further discussed in the next problem.

Now suppose we wish to design a current controlled voltage source (CCVS) of a transimpedance R ($v_{out} = Ri_{in}$, output impedance is small and ouput impedance is small). Starting from the circuit shown in figure 3, using a resistor of value R and a transconductance g_m (which is large compared to $\frac{1}{R}$), derive a transistor level circuit for the CCVS with as few transistors as possible.

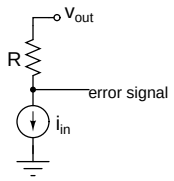


Figure 3: Synthesizing a CCVS

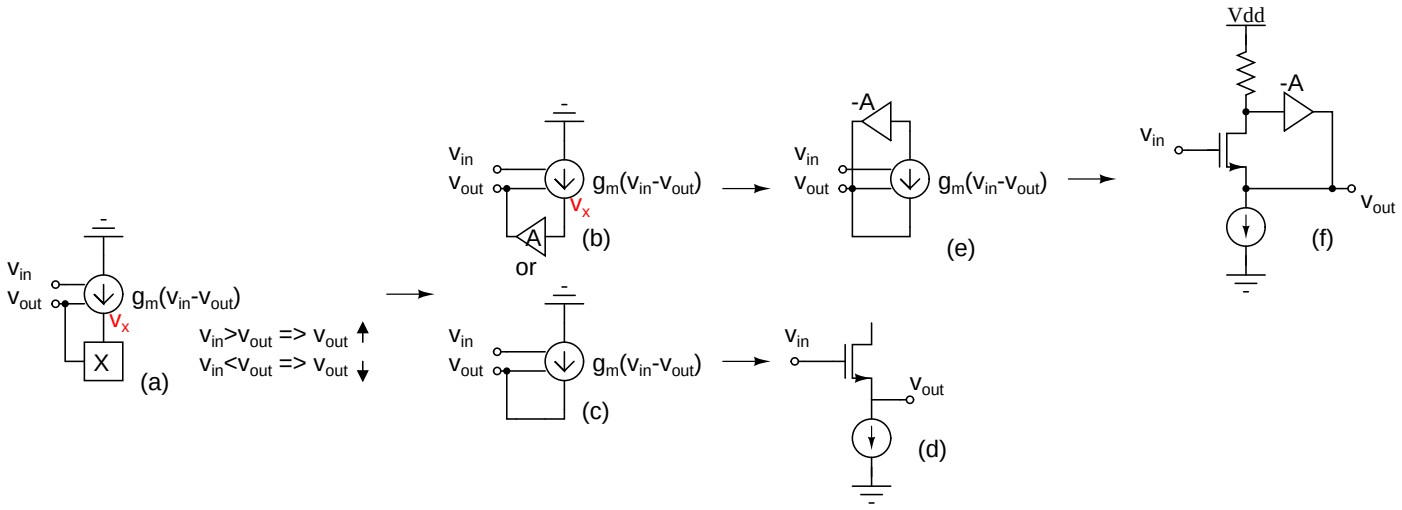


Figure 2: Synthesis of a Voltage controlled voltage source (VCVS) network

4 Problem 4

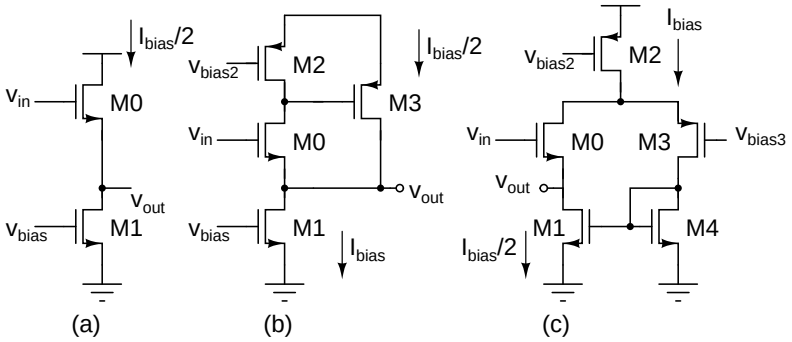


Figure 4: Compairson of different voltage buffers

In this problem, we investigate different topologies to build a voltage controlled voltage source. As seen from the previous problem, starting from small signal circuits, one can derive a variety of transistor topologies to implement a given small signal transfer function and many more topologies with the same small signal equivalent circuit but different biasing mechanisms. Consider the three topologies shown in figure 4. In all the three schemes, the devices marked M0 carry $\frac{I_{bias}}{2}$. The last two of the three are such that they consume the same amount of power. Assuming g_{mn}, r_{on}stand for the transconductance and the output impedance of the nMOS transistor and that $g_{mn}r_{on} \gg 1$ and similar definitions for the pMOS transistors, derive the small signal output impedances of the circuits. Make reasonable assumptions whereever necessary and justify them. What do you observe about the ouptput impedances? Identify the amplifier block (marked as -A) by comparing the topologies with the figure 2(f). Apart from the difference in headroom, what have we traded for better output impedance (in the topologies with lower output impedance)?