

EE6312 Project

Spring 2009

March 31, 2009

The goal of this project is to design a switched capacitor input stage of a pipelined A/D converter including the opamp, MOS switches and capacitors.

System spec

Design one stage of a pipelined ADC working at the sampling speed you have chosen and for the resolution you have chosen. There are 16 combinations available and you can work in groups of two.

Background

A basic block diagram of a stage in a pipelined A/D converter is shown in figure 1

The entire circuit (and hence the opamp) has to be fully differential. It will be driving a switched capacitor circuit. Typically the contents of the dashed area in figure 1 might contain something as shown in figure 2. Note that this is just an example and the literature you will refer to might not contain a stage identical to this. There could be many different implementations of this block - each having its own advantages w.r.t sampling, charge injection, parasitics, offset etc. You do not have to use this circuit.

This circuit will be driving the next stage in the pipeline and so on. B and \bar{B} in the circuit are outputs of the A/D converter which is outside the dashed region. One might choose to use a 1 bit A/D (also known as a comparator) and a 1 bit D/A in one stage of the pipeline converter.

For your own understanding, you have to first analyze the block diagram (figure 1) and see for yourself how a pipelined A/D works. You will realize that the accuracy of the complete A/D converter with all of its stages is completely defined by the accuracy of the dashed area of the first stage of the pipelined converter. Now, for your own understanding analyze the circuit (figure 2) shown and see that indeed it does fit into the dashed area of the block diagram. The goal of this project is to design this dashed region of the block diagram.

References

For further reading on pipelined A/D Converters, or to get a clear understanding, please refer to the following papers:

1. "A pipelined 5-Msample/s 9-bit analog-to-digital converter," S. H. Lewis & Paul Gray: JSSC Dec. 1987
2. "A 12-bit 1-Msample/s capacitor error-averaging pipelined A/D converter," Song, Tompsett & Lakshmikumar: JSSC Dec. 1988
3. You can also refer to Johns and Martin, Analog Integrated Circuit Design, Chapter/Section 13.5, 13.8 for a very brief introduction on pipelined ADCs.
4. For fundamentals on A/D conversion, definitions etc, refer to Johns and Martin, Analog Integrated Circuit Design, Chapter 11.

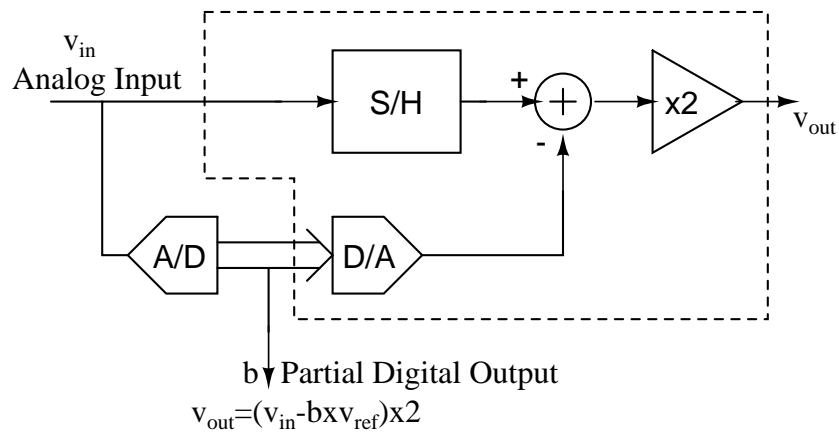


Figure 1: Block diagram of a stage in a pipelined ADC

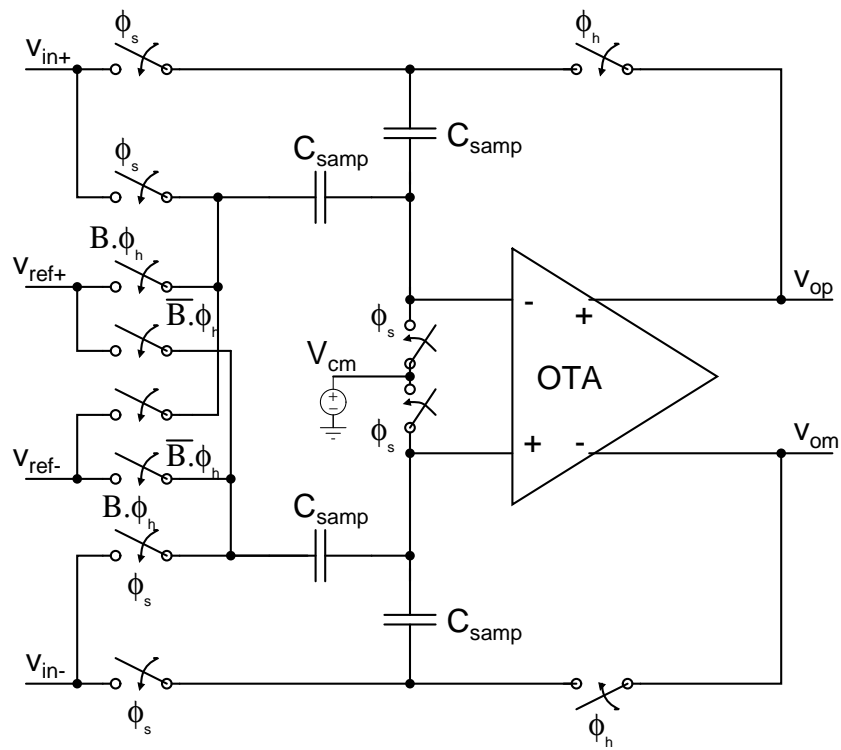


Figure 2: One implementation of a pipelined ADC stage

Notes

1. Design the input stage of the pipelined ADC assigned to you. Choose the sampling capacitor such that the size of the least significant bit is at least 4x the rms $\frac{kT}{C}$ noise due to the sampling capacitor. Choose T to be 300 K. If you happen to not know how this comes about, just assume that you need to calculate the capacitor value from this condition. The term k here refers to the Boltzmann constant.
2. Make sure that you get settling correct within $\frac{LSB}{4}$ when you input a sine wave of frequency $\frac{f_s}{2}$ of full-scale amplitude or a square wave of frequency $\frac{f_s}{2}$ toggling between V_{fs} and $-V_{fs}$.
3. As an input source you can use a voltage source; as a load assume a similar stage as your own stage. Keep in mind the requirement this imposes: the input and output common mode voltages need to be equal!
4. You HAVE to use the Teaching model.
5. The goal is to design your opamp for **minimal** power consumption for your specifications (Indirectly, the least FOM defined below).
6. Design for a nominal V_{dd} should be 1.8V.
7. You can assume you have an ideal 1-bit comparator with a maximum offset of 3 mV. Use the cell "switch" in "analogLib" to simulate this.
8. The design has to be **Fully Differential**.
9. You need to design the opamp, capacitors and switches only. You can assume you have voltage references, comparators, clock generators. You can use the analogLib source vpulse to generate all your clocks; otherwise, for a simple non-overlapping clock generator refer to figure 10.3 in Johns and Martin.
10. You need to simulate your circuits and tabulate the performance over different process (ss, tt, ff), supply (1.6 V, 1.8 V, 2.0 V) and temperature (0degC, 100degC) corners; at the least you have to simulate the worst (ss, 1.6V, 100degC), typical (tt, 27degC, 1.8V) and best (ff, 0degC, 2.0V) cases. For this project, it is ok if your circuit only meets the specifications at the typical conditions. You don't have to redesign the circuit to meet the specs under all conditions.
11. We suggest to use OCEAN scripts to automate the simulations but it is not required. It is especially useful while doing corner simulations.

Design Procedure:

1. System Level Design: (Time allotted: finish by Apr 12)
 - (a) Choose a reasonable value for VFS and calculate the size of VLSB. Also, determine Vref. What constitutes a reasonable VFS or LSB size?
 - (b) Determine the opamp specifications using the ideal opamp model given below (gain, bandwidth, phase margin) based on settling requirements.
 - (c) Use the opamp model and ideal switches and see if your design will work.
 - (d) Derive the transfer function for the switched capacitor gain block taking into account CP, the opamp input capacitance, and a single pole transfer function for the op-amp.
 - (e) Now assume an ideal opamp (very large Gain-Bandwidth (GBW) and gain), and design the switches. Pay attention to the switch resistance Rsw and the charge injection.
 - (f) Choose the switch MOSFET size.
2. At this point get your circuit verified. Opamp Design: (Time to allot: finish by Apr 19)
 - (a) Design an opamp that satisfies these requirements; choose the topology; size transistors; verify specs.

- (b) A reference for a possible opamp architecture to start from can be found in: Fully Differential Operational Amplifier with Accurate Output Balancing - Mihai Banu, John Khoury, Y. Tsvividis, IEEE JSSC Dec. 1988 page 1410-1414.
 - (c) Make sure that the input referred noise is of the same order of magnitude as the noise of the switch.
 - (d) Pay a lot of attention to the design of the common mode feedback circuit for your opamp that has sufficient bandwidth as well as phase margin.
3. At this point, if you are unable to reach the specs as decided by phase I of your project, try to change the parameters in phase I till you reach opamp specs you can achieve. If you do change the specs, consult the TA for a sanity check. If you need any kind of help with the opamp design, do not hesitate to approach the TA. Overall A/D stage simulations: (Time to allot: finish by Apr 26)
- (a) Plug in the opamp in the A/D stage with MOSFET switches and run through clock phases; prove the 2x amplification happens with the right accuracy; show that you have enough settling time, etc.
 - (b) You need to show results for the following two cases atleast: i) Apply at the input a small signal going from 1 LSB to -1 LSB and back to 1 LSB. ii) Apply large signal, going from Full-scale Voltage (V_{fs}) input voltage to $-V_{fs}$ back to V_{fs} .
 - (c) Tabulate your results for slowest (ss process, 1.6V and 100 C), fastest (ff process, 2.0V and 0 C) and typical (tt process, 1.8V and 27 C) corners.
4. Write the report (see below for the required format).

Final report format:

- You will be graded based on the figure of merit (FOM) of your design. $FOM = \frac{\text{Power}}{2^{ENOB} f_s}$ where ENOB is defined as $\frac{\text{SINAD} - 1.76}{6.02}$ (SINAD stands for Signal to Noise and Distortion ratio). As you can see, doubling the sampling speed should result in doubling of power for the same FOM. Similarly, increasing the no. of bits by 1 should require twice the amount of power. This would therefore result uniform level of difficulty for everyone.
- You should hand in a brief Journal of Solid State Circuits style report. Remember that although you would be graded on the FOM you achieve, your report is what gives the TA a fair idea of your effort. Try to make it as detailed as possible keeping its length below six pages of text. It should also contain all circuit schematics, simulation plots that you want the professor/grader to see. (LaTeX style files http://www.ieee.org/portal/cms_docs/pubs/transactions/IEEEtran.tar.gz, Microsoft Word author's template http://www.ieee.org/portal/cms_docs/pubs/transactions/TRANS-JOUR.DOC.)
- You should tar/gzip your design library so that in case we need to check, we can rerun the required simulations. Have a file called "README" inside the tar/gzip of your database which essentially describes what is what and gives pointers to how to do important simulations.
- Simulation results should include (but are not restricted to) opamp differential frequency response (indicating dc gain, bandwidth, phase margin); transient differential and common mode step response for an input step of amplitude V_{LSB} and for an input step of amplitude V_{fs} ; opamp common mode frequency response; transient simulations in the overall A/D converter stage including the opamp, capacitors and switches.
- Submit by May 3rd.