BARADWAJ VIGRAHAM

CONTACT INFORMATION

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INTERESTS

Analog/Mixed signal/RF Integrated circuit design

EDUCATION

Columbia University, New York *August 2008 - Present*

- Doctoral track program (M.S-Ph.D) in Analog/RF IC design
- Grade Point Average: 4.05/4.00 (as of Spring 2010)
- Master of Science (M.S) degree awarded in February 2010

Indian Institute of Technology Madras (IIT Madras), Chennai, India *August 2004 - April 2008*

- Bachelor of Technology (B.Tech) in Electrical Engineering
- Minor in Physics
- Cumulative Grade Point Average: 9.23/10

CURRENT RESEARCH

- **Switched-Mode Signal Processing:** Developing a new analog/mixed signal design paradigm geared towards high performance (> 60 dB SNDR, ≈ 100 MHz applications) and a *digital-friendly* approach.
- **Ultra-wide-band transceiver design for ultra-low power sensor networks:** We are targetting close to 100 μW power consumption for > 10 m NLOS communication, while supporting 3-channels for FDMA, in the lower UWB band (3-5 GHz).

RESEARCH EXPERIENCE

- Developed a new signal processing paradigm, switched-mode signal processing for high-performance analog/mixed signal circuit design. Three projects were proposed as demonstration vehicles and was awarded an **NSF grant (Switched-Mode Signal Processing: An Innovative Paradigm for High Performance Analog in Nanoscale CMOS, Award# 1309721**, PI: Peter Kinget**)**

- Developed a low area passive phase shifter for millimeter wave radio as an intern at Kilby Labs, Texas Instruments, Dallas in the summer of 2011
- As an intern at Silicon Labs, Austin, TX in the summer of 2010, an investigative attempt to integrate active splitters with existing TV tuners for Picture-in-Picture applications. The primary challenge lies in the design of a highly linear ($\geq$ 25 dBm IIP3) LNA in Silicon on a 2.7 V supply. A novel, highly process tolerant distortion cancelling technique was proposed for this purpose.
- Worked as an intern at Silicon Labs, Austin, TX in the summer of 2009. It primarily involved comparing 130nm and 65nm technologies and moving a PLL to the 65nm technology as a test structure for their future designs.
- Designed a 1 GHz sampling rate, 4-bit flash ADC with sub-nano second delay for use in a continuous time $\Sigma - \Delta$ modulator in 180nm technology towards my undergraduate thesis.
- In an internship at Texas Instruments India, I analysed the validity of various approaches used to study the stability of feedback systems and applied it to understand the reasons for the instability in one of the LDRs (Low drop-out regulators) being designed by them.

AWARDS

- Was awarded the Armstrong Memorial Award for M.S students by the Electrical Engineering department at Columbia University for outstanding performance. *2009-2010*
- Was awarded the Analog Devices Outstanding Designer Award by Analog Devices Inc. *2012-2013*

TEACHING

- Teaching assistant for Introduction to Electrical Engineering *Fall '08*
- Teaching assistant for Advanced Analog Integrated Circuits *Spring '09*

PUBLICATIONS *(chronologically)*

- **B. Vigraham**, P. Kinget, "A Self-Duty-Cycled and Synchronized UWB Pulse-Radio Receiver SoC with Automatic Threshold-Recovery Based Demodulation", IEEE Journal of Solid State Circuits (JSSC), *In Review*
- M. Gorlatova, R. Margolies, J. Sarik, G. Stanje, J. Zhu, **B. Vigraham**, M. Szczodrak, L. Carloni, P. Kinget, I. Kymissis, G. Zussman, "Prototyping Energy Harvesting Active Networked Tags (EnHANTs)", in Proc. IEEE INFOCOM'13 mini-conference, Turin, Italy, Apr. 2013.
- **B. Vigraham**, P. Kinget, "A Self-Duty-Cycled and Synchronized UWB Receiver SoC Consuming 375pJ/b for -76.5dBm Sensitivity at 2Mbps," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2013
- V. Singh, N. Krishnapura, S. Pavan, **B. Vigraham**, D. Behera, N. Nigania, "A 16MHz BW 75dB DR CT $\Delta\Sigma$ ADC compensated for more than one cycle excess loop delay," IEEE Journal of Solid State Circuits (JSSC), Aug. 2012
- **B. Vigraham**, P. Kinget, "An Ultra Low Power, Compact UWB Receiver with Automatic Threshold Recovery in 65 nm CMOS," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Jun. 2012
- G. Stanje, P. Miller, J. Zhu, A. Smith, O. Winn, R. Margolies, M. Gorlatova, J. Sarik, M. Szczodrak, **B. Vigraham**, L. Carloni, P. Kinget, I. Kymissis, and G. Zussman, Demo: Organic solar cell-equipped energy harvesting active networked tag (EnHANT) prototypes, in Proc. ACM SenSys11, Nov. 2011
  - Received the best student demo award
- V. Singh, N. Krishnapura, S. Pavan, **B. Vigraham**, N. Nigania, D. Behera, "A 16MHz BW 75dB DR CT $\Delta\Sigma$ ADC compensated for more than one cycle excess loop delay," IEEE Custom Integrated Circuits Conference, Sep. 2011
- J. Zhu, G. Stanje, R. Margolies, M. Gorlatova, J. Sarik, Z. Noorbhaiwala, P. Miller, M. Szczodrak, **B. Vigraham**, L. Carloni, P. Kinget, I. Kymissis, and G. Zussman, "Demo: Prototyping UWB-Enabled EnHANTs", Proc. ACM MobiSys'11, Washington, DC, Jun. 2011