

EE6312 Project, Spring 2010

Instructor Prof. Harish Krishnaswamy
TA: Karthik Tripurari

April 11, 2010

1 Projective Objective

- The goal of this project is to design a switched capacitor 1-bit input stage of a pipelined A/D converter. It involves the design and integration of opamp and MOS switches.
- The sampling frequency should be one of the following - 10 MS/s, 20MS/s, 30MS/s, 40MS/s and resolution should be between 6 bits to 10bits.

2 Guidelines for Design

- Sampling capacitor is chosen such that the size of the least significant bit is at least 4 times the rms $\frac{kT}{C}$ noise due to the sampling capacitor. Choose T to be 300 K.
- Settling error should be within $\frac{V_{LSB}}{4}$ when a sine wave of frequency $\frac{f_s}{2}$ of full-scale amplitude is given as input. Gain and bandwidth of the opamp are determined by this condition.
- V_{LSB} and V_{ref} are to be determined by the designer.
- After calculating the required gain and bandwidth of the opamp, a verification is recommended to check if the settling error is lesser than $V_{LSB}/4$. A model of opamp built using analogLib vcvs is sufficient for this verification. Transistor level design of the opamp should be done after finalizing the gain and bandwidth requirements.
- Only the opamp, capacitors and switches need to be designed in this project. Ideal voltage references, comparators, clock generators can be used. Analoglib vpulse source can be used to generate all the clock phases.
- A sub-ADC (1-bit) block is required to simulate the pipelined converter stage. An ideal block could be used for this purpose.

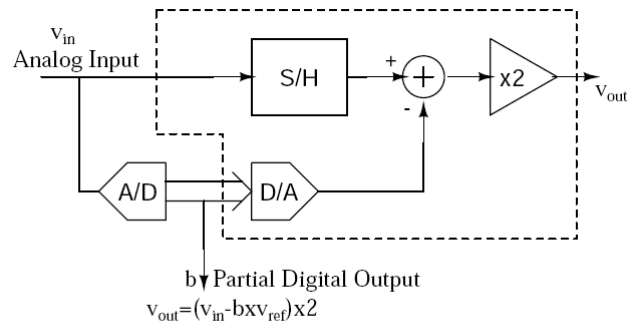


Figure 1: Block diagram of a stage in a pipelined ADC

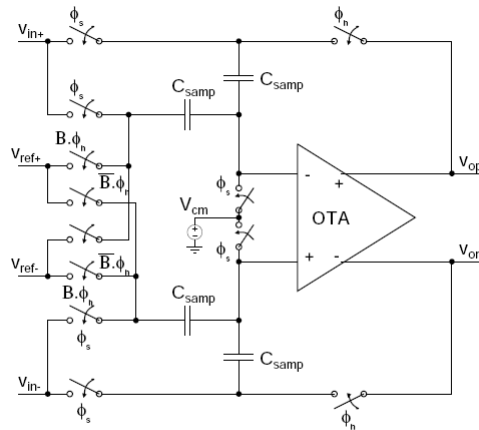


Figure 2: One implementation of a pipelined ADC stage

- One ideal current source can be used and all the other currents should be generated by using current mirrors.
- A 2Ω resistance should be added in series with the power supply in all the simulations.
- The opamp will be driving a load similar to the designed stage. Load for the opamp is decided based on this.
- The TSMC018 Teaching model has to be used.
- The Vdd should be 1.8V.

3 Evaluation criterion

The final project will be evaluated on the performance of the stage and final report. Performance of the design is judged based on a Figure of Merit (FOM), which is given by,

$$FOM = \frac{P}{2^N f_s}$$

where P is the power consumed, f_s is the sampling frequency and N is the effective number of bits of the ADC calculated based on the SNR at the output. Since only a single stage of a pipe-line is being designed, N can assumed to be equal to the desired number of bits of the ADC, provided the settling error is lesser than $V_{LSB}/4$.

4 Final Report

The final report should include

- A neat schematic of the opamp, showing all component sizes and values.
- Bodeplot demonstrating the bandwidth and the phase margin of the opamp.
- A transient response demonstrating stability of the opamp.
- A table of important parameters (gain, bandwidth, slew rate, settling time, power) of the opamp.

The report needs to focus on the design procedure that was followed, the trade-offs considered, steps taken to optimize power consumption, reason for the choice of circuit topology etc. Grading is not entirely based on the performance of the design, but also on explanation of design techniques used to achieve the reported results or the design challenges that impeded further improvement of the performance.

5 Guidelines for final Submission

- Please tar your cadence schematics and test benches with saved simulation setup states in cellview format. A README file which states what is included and how to rerun the important simulations should also be in the tar file.
- Cadence plots and schematics usually do not look clear on reports. You could use xccircuit for making schematics and matlab for plotting.
- The length of the report should not exceed six pages. It should contain all circuit schematics, mention sizes of all components and include important simulation plots. The figures and the tables should be at the end of the report, and large enough so everything is readable. A clear, concise and well-written report is key to receiving a favorable grade.

6 References

- “A pipelined 5-Msample/s 9-bit analog-to-digital converter,” S. H. Lewis, Paul Gray: JSSC Dec. 1987.
- “A 12-bit 1-Msample/s capacitor error-averaging pipelined A/D converter,” Song, Tompsett, Lakshmikumar: JSSC Dec. 1988.
- You can also refer to Johns and Martin, Analog Integrated Circuit Design, Chapter/Section 13.5, 13.8 for a very brief introduction on pipelined ADCs.
- For fundamentals on A/D conversion, definitions etc, refer to Johns and Martin, Analog Integrated Circuit Design, Chapter 11.