Columbia University
EE6314 Fall 09 Project

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TA : Karthik Tripurari Jayaraman

1 General Information

1.1 Objective

- To gain design experience of key RF building blocks - LNA, Mixer, VCO and LO Buffers.
- To become comfortable with advanced RF circuit simulations.
- To gain familiarity with RF system specifications.
- To practice writing in engineering field.

1.2 Project Overview

The assignment of this project is to design a single dual-band RF front-end direct conversion receiver circuit for GSM-900M and GSM-1800M communication systems. The block diagram of the receiver is as shown in Fig. (1).

1.3 Design Goal

To achieve minimum power consumption while meeting all the design specifications for typical process and operating conditions.

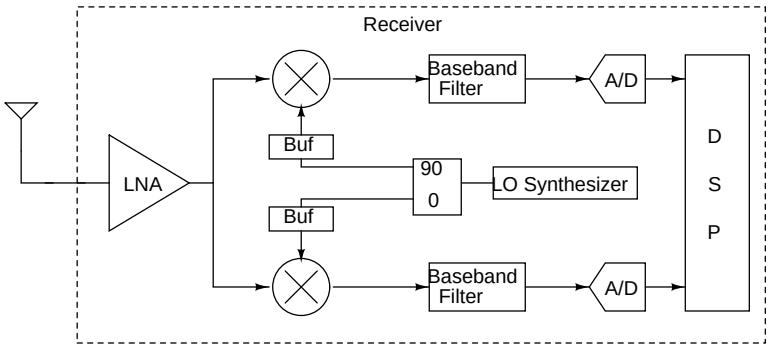
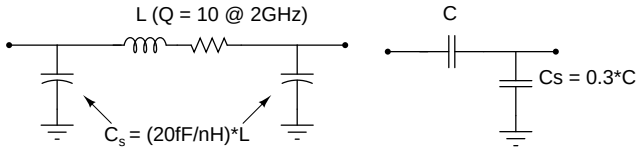


Figure 1: A RF Transceiver

Figure 2: More realistic models for Passives



(a) Model for Inductor (b) Model for Capacitor

1.4 Supply Voltage and Process

VDD: 1.8 V
Process: TSMC 0.18um CMOS
The models are available in VLSI lab machines in /work/tools1/tech/tsmc018/tsmc018/T-018-MM-SP-002/fp1/spectre445. It only includes the models for nmos and pmos transistors. Use the model in Fig. (3(a)) and Fig. (3(b)) for inductors and capacitors respectively. If you need varactors, use inversion-mode MOS varactors.

1.5 Simulations

Your design needs to meet all specifications for typical process and operating conditions. But in addition you need to do all simulations in the following three cases and show the performance of your design against the given specifications:

- Typical case: tt (typical corner), Temp=27C and VDD=1.8V.
- Worst case: ss (slow corner), Temp=85C, VDD=1.6V.
- Best case: ff (fast corner), Temp=-20C, VDD=2V.

Variations in performance across PVT (process, voltage, temperature) are to be expected, but if your design exhibits substantial variation, you should verify.

1.6 Groups

You may work either individually or in a group of 2 students. Discussion with others is encouraged but genuine design work from each group is required. All sources used need to be properly referenced or acknowledged in your research report. Make sure to interact regularly with the TA during office hours on your progress, ideas and challenges.

1.7 Deadlines and Deliverables

- Part 1 LNA : November 13th.
- Part 2 Mixer + LO Buffers : November 30th.
- Part 3 LNA + Mixer + LO Buffers : December 14th.
- Part 4 Final Submission: December 17th.

The deadline for final submission is fixed and can not be changed. The grading is based only on the final submission. Though the other deadlines are flexible, you are strongly recommended to adhere to stick to this schedule. From our past experience, students who have followed the schedule have done better.

After every stage, it is recommended that you characterize and document your design. The documentation should include

- Transistor level schematics of the design. Tabulate all the component values and transistor sizes.
- Top-level schematics for all test setups. Create symbols for your LNA/Mixer/Buffer and then create top-level test benches.
- Simulation plots for typical case.
- Simulation results in a table for all three corners.

1.8 Final Submission

1. Please tar your cadence schematics and test benches with saved simulation setup states in cellview format. A README file which states what is included and how to rerun the important simulations should also be in the tar file.
2. For your report, please arrange all simulation plots and tabular results in one PDF file, briefly explain/comment when appropriate. Cadence plots and schematics usually do not look clear on reports. You could use xcircuit for making schematics and matlab for plotting. Do not print pages of simulations and schematics, but rather select the key simulations to show and extract key performance metrics and organize them.
3. Performance summary of the individual blocks and overall design in a datasheet. Tabulate Noise Figure, IIP3, IIP2, P-1dB, Gain, S11, 1/f noise corner and Power Consumption for each band. Also tabulate the flatness of Gain and Noise figure in the bands 880MHz-960MHz and 1710MHz-1890MHz.
4. Make a spreadsheet of your receiver design, including noise figure and linearity calculation.
5. A level diagram of the receiver based on the spreadsheet you made, refer to the example in the lecture notes.
6. The transient simulation results of the input and output terminals of LNA, Mixer and VCO need to be plotted for
   (a) RFin at 1801MHz and LOin at 1800MHz.
   (b) RFin at 901MHz and LOin at 900MHz.
7. For the VCO design (optional), you need to submit the following simulation results:
   (a) Frequency Tuning Curve: LO frequency versus tuning voltage.

(b) Phase Noise versus Offset Frequency

(c) Table of tuning gain of VCO, gain/phase error in signals at the input of LO buffers of RC/CR network (at 1.7GHz, 1.8GHz and 1.9GHz) and power consumption at all temperatures and corners.

(d) Figure of Merit for the VCO

$$FoM = 10log_{10}\left(\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\}P}\right) \quad (1)$$

where f_0 is 1.8GHz/3.6GHz depending on your choice of oscillator, Δf is 1MHz, $L\{\Delta f\}$ is phase noise at that offset and P is the power consumed by the oscillator.

You need to hand in a clear report. It should allow the educated reader to understand how the design was performed. The report needs to focus on the design procedure that you followed. Make sure to include the trade-offs considered, steps taken to optimize power consumption, reason for the choice of circuit topology etc. You are not graded based only on the performance of your design, but also on explaining what design techniques you used to achieve the reported results or what design challenges limited you from further improving the performance.

The length of the report should not exceed six pages (not including figures/tables). It should contain all circuit schematics, mention sizes of all components and include important simulation plots. The figures and the tables should be at the end of the report, and large enough so everything is readable. A clear, concise and well-written report is key to receiving a favorable grade.

2 System Requirements

Table 1: Requirement for the receiver

Standard	Noise Figure (dB)	IIP3 (dBm)	S11 (dB)	Conversion Gain(dB)	1/f corner
GSM900M	< 7	> -15	< -10	> 30	$10k$
GSM1800M	< 7	> -15	< -10	> 30	$10k$

Notes

- For performing the two tone test to measure IIP3, we need two tones such that their inter-modulation product falls in the channel. Use the information in the Table (2).

	Channel	Tone I	Tone II
GSM900MHz	950M-950.2M	950.6MHz	951.1MHz
GSM1800MHz	1850M-1850.2M	1850.6MHz	1851.1MHz

Table 2: Information for the two tone test

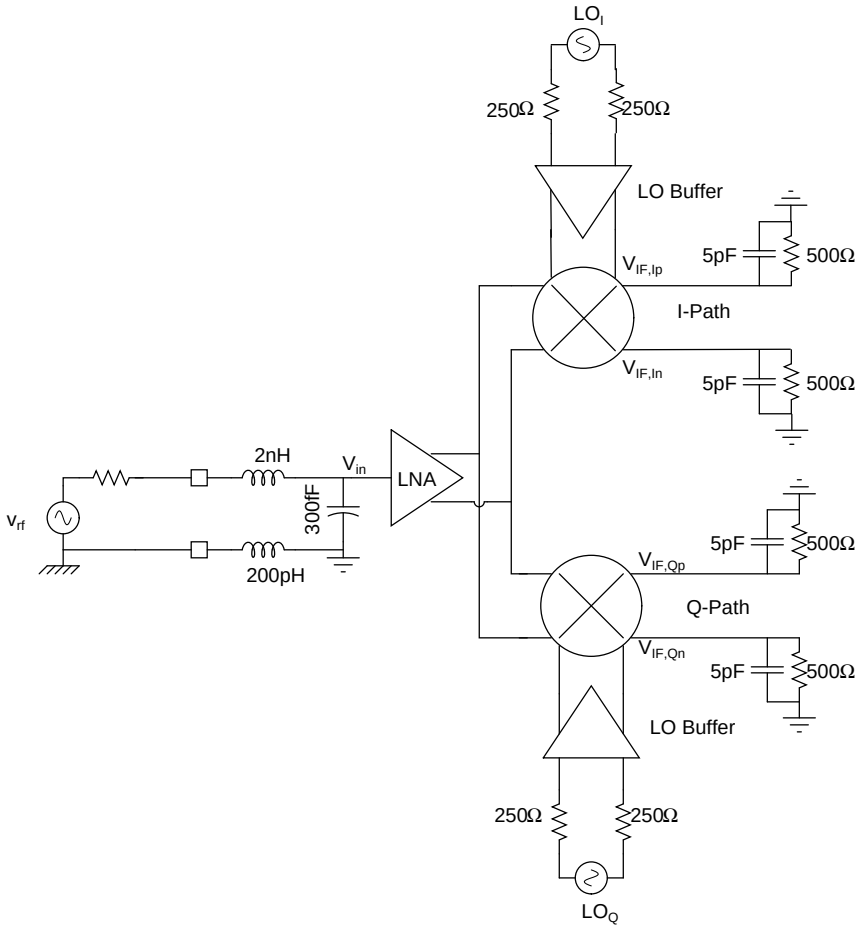


Figure 3: Testbench for the System

- Conversion gain is given as

$$CG = \frac{V_{IF,Ip} - V_{IF,In}}{V_{in}}$$

- Due to the presence of 1/f noise, the spectral density in the channel bandwidth is not flat and the usage of spot noise to calculate noise figure is not correct. Instead, you should use the noise integrated over the channel bandwidth and use this to calculate the noise figure.
- Your chip needs to have a single ended RF interface and differential baseband outputs. A transformer or balun (on-chip or off-chip) cannot be used for single ended to differential conversion.
- At RF input a $2mm$ bond-wire (modeled as a 2nH inductor) and a bondpad (modeled as a 300fF capacitor) need to be taken into account for the LNA design.
- Your RF input needs an impedance match to a 50Ω source impedance.

3 How to get started?

The following subsections give an idea of where to start. The final goal is to meet the overall requirement of the receiver and not for individual blocks. Expect that a few iterations may be required before you meet the specifications.

3.1 LNA (see Fig. (4))

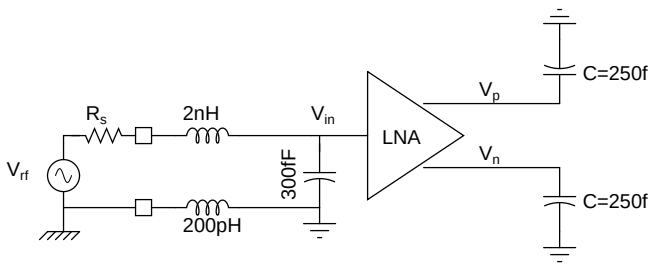


Figure 4: Testbench for a LNA

- NF <2.5 dB
- Voltage Gain ($\frac{V_p - V_n}{V_{in}}$)> 15dB
- IIP3 > -2dBm
- S_{11} < -10dB

For this initial design assume that the LNA is driving 250fF loading capacitance. This loading capacitor models the gate capacitance of the mixer stage that you will design later. Note that the LNA specifications given here are just a starting point. When you put together the LNA and the mixer, you will need to modify the design to get the specifications right and optimize the performance.

3.2 Mixer and LO Buffers (see Fig. (5))

- Voltage Conversion Gain ($\frac{IF_p - IF_n}{RF_p - RF_n}$) > 15dB.
- IIP3 > 3dBm
- Assume LO = 300 mVpp (input at LO_{in})
- Assume 1% mismatch (in W/L) for the LO and RF differential mixer pairs (if this cannot be directly applied to your chosen mixer topology, consult with the TA how to introduce device mismatch in your design).

The impedance of the source that drives the mixer is the impedance seen from your LNA output. Measure the differential output impedance 2Rs of your LNA and model it as the impedance of the signal source driving your mixer at the frequency range of interest. The single ended output load of the mixer is $5pF||500\Omega$. For the LO buffer design you can assume a 250Ω single-ended VCO output impedance.

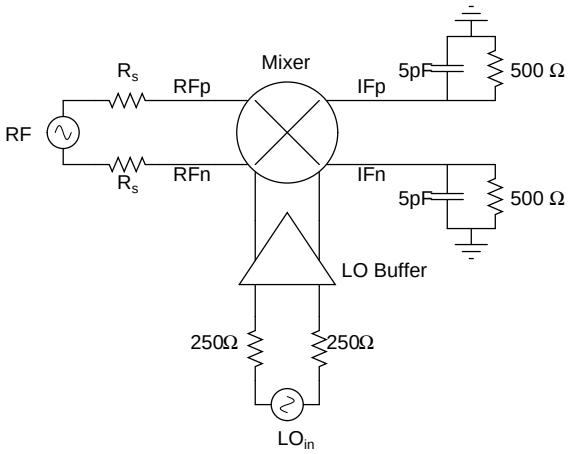


Figure 5: Testbench for a Mixer

Don't restrict yourself to the switching mixer which was analyzed in detail in the class. Explore other architectures like passive mixers as well. Some references are available on the website.

3.3 VCO (Optional)

We need quadrature LO at 900MHz and 1.8GHz. You could use one of the two following techniques.

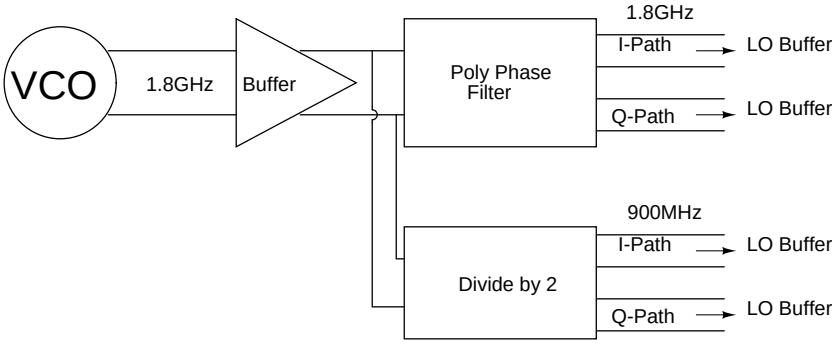
3.3.1 Method One (see Fig. 6(a))

- Design a VCO that oscillates at 1.8GHz with a tuning range of ±10%.
- Use a RC-CR network to generate quadrature @ 1.8GHz. You are free to use more complicated quadrature generation schemes. How much error do observe in quadrature phase when you operate at the end of tuning range?
- Use a divide-by-2 circuit to generate 900MHz signal. Quadrature phases are available when a divide-by-2 operation is performed.

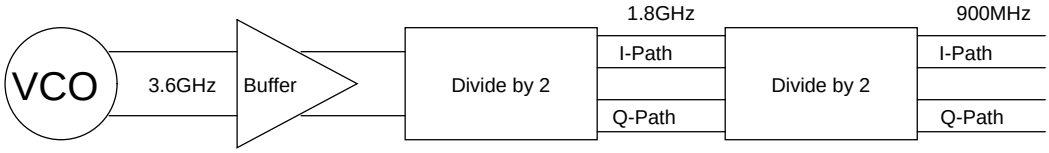
3.3.2 Method Two (see Fig. 6(b))

- Design a VCO that oscillates at 3.6GHz with a tuning range of ±10%.
- Use a cascade of divide-by-2 circuits to generate the necessary frequencies.

You can start with a differential LC oscillator topology. You need to use the inductor and capacitor models provided for this project. Use inversion mode MOS varactors for your design. Include switched capacitors in your LC tank or increase the tuning range provided by the varactor to compensate the frequency changes due to process variations. If you use a combination of varactors and switched capacitors for tuning, make sure that the tuning range provided by the varactors is at least ±3%.



(a) 1.8 GHz VCO



(b) 3.6 GHz VCO

Figure 6: Testbench for VCO