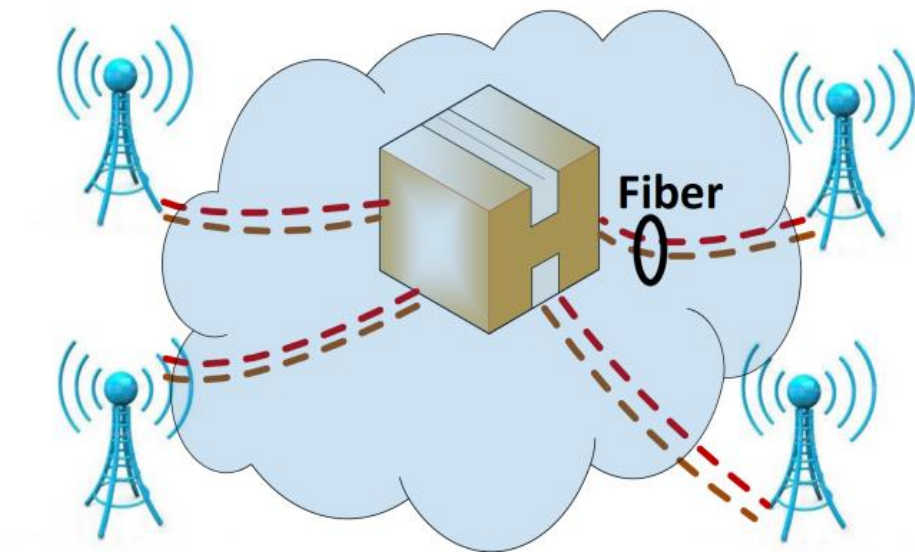# Massive Millimeter-wave MIMO for 100G Wireless

Anandaroop Chakrabarti, Mehdi Ashraphijuo, Harish Krishnaswamy and Xiaodong Wang
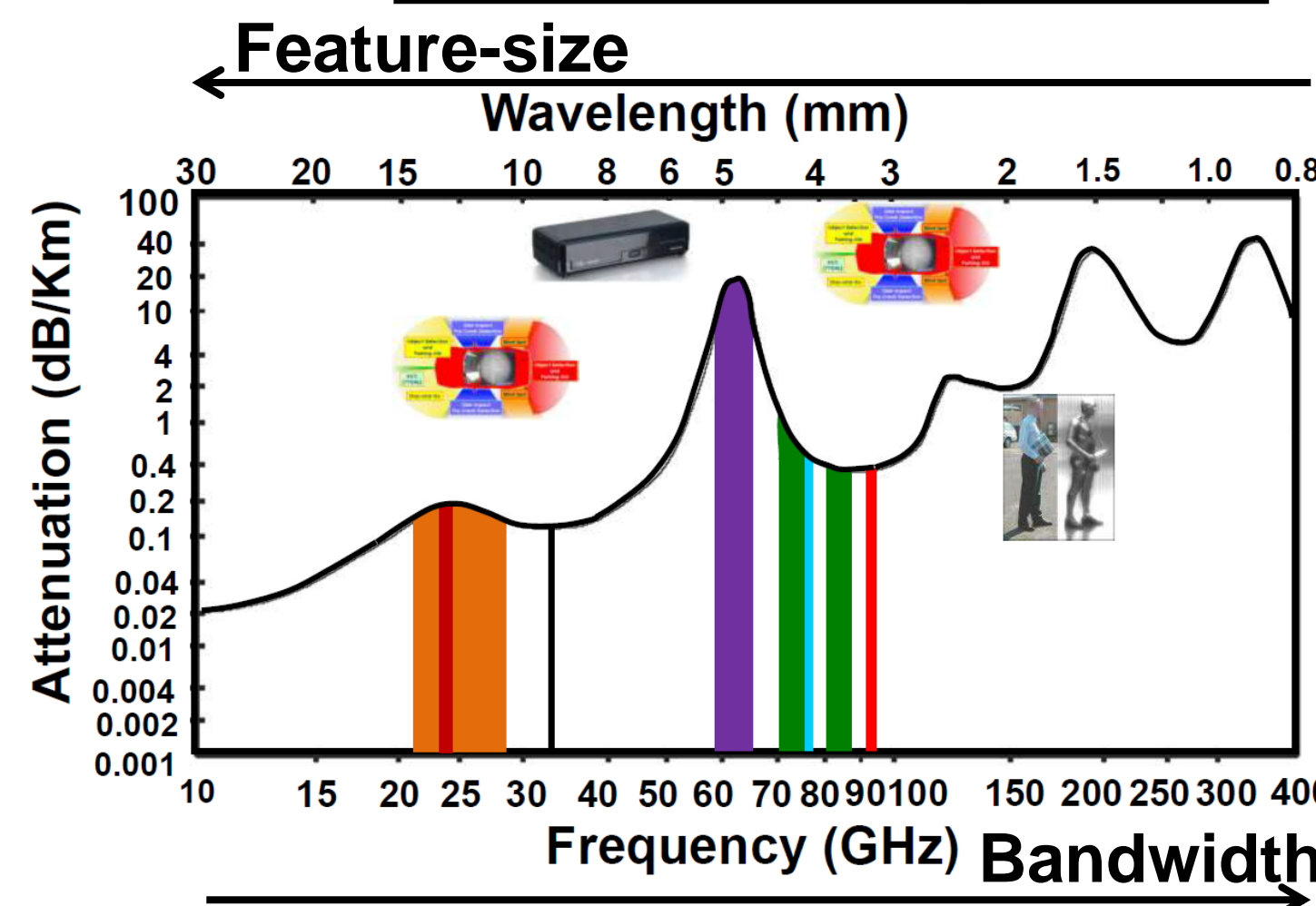
Motivation

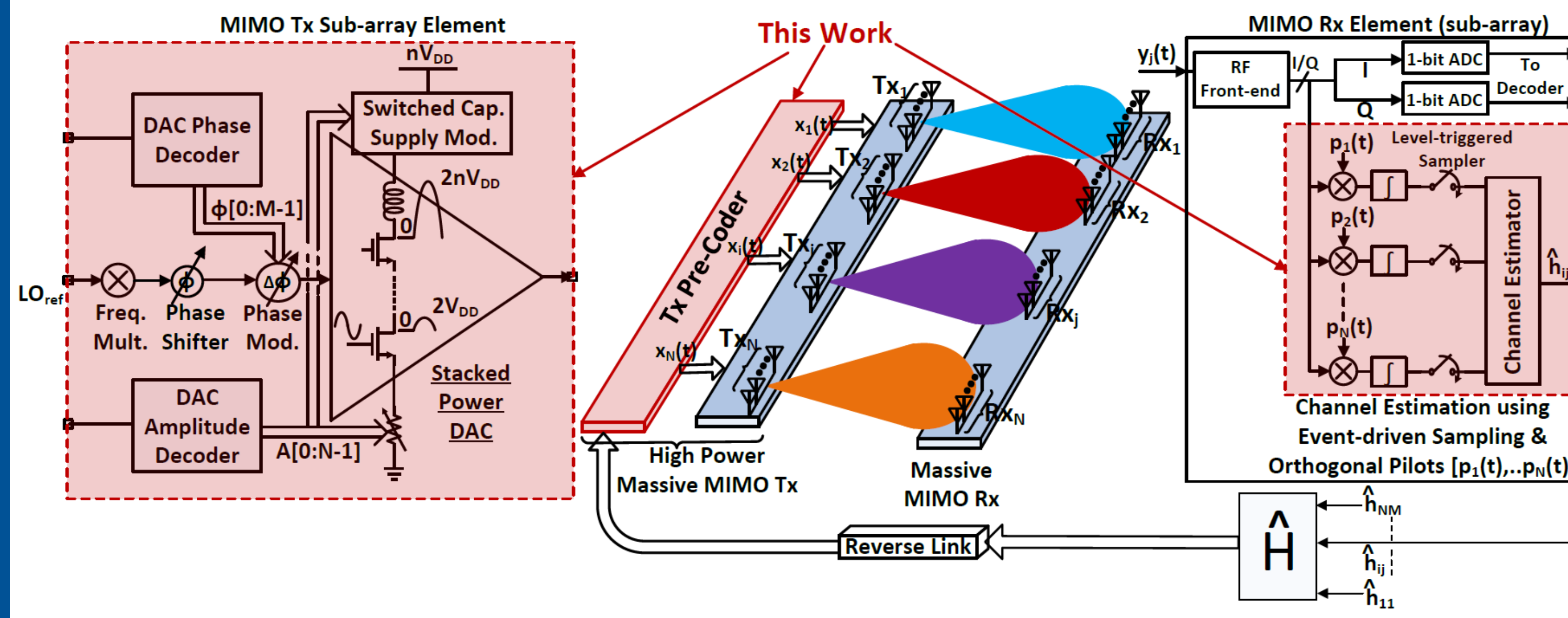### The Mobile Backhaul Problem

Fiber

- High initial investment.
- High repair cost.
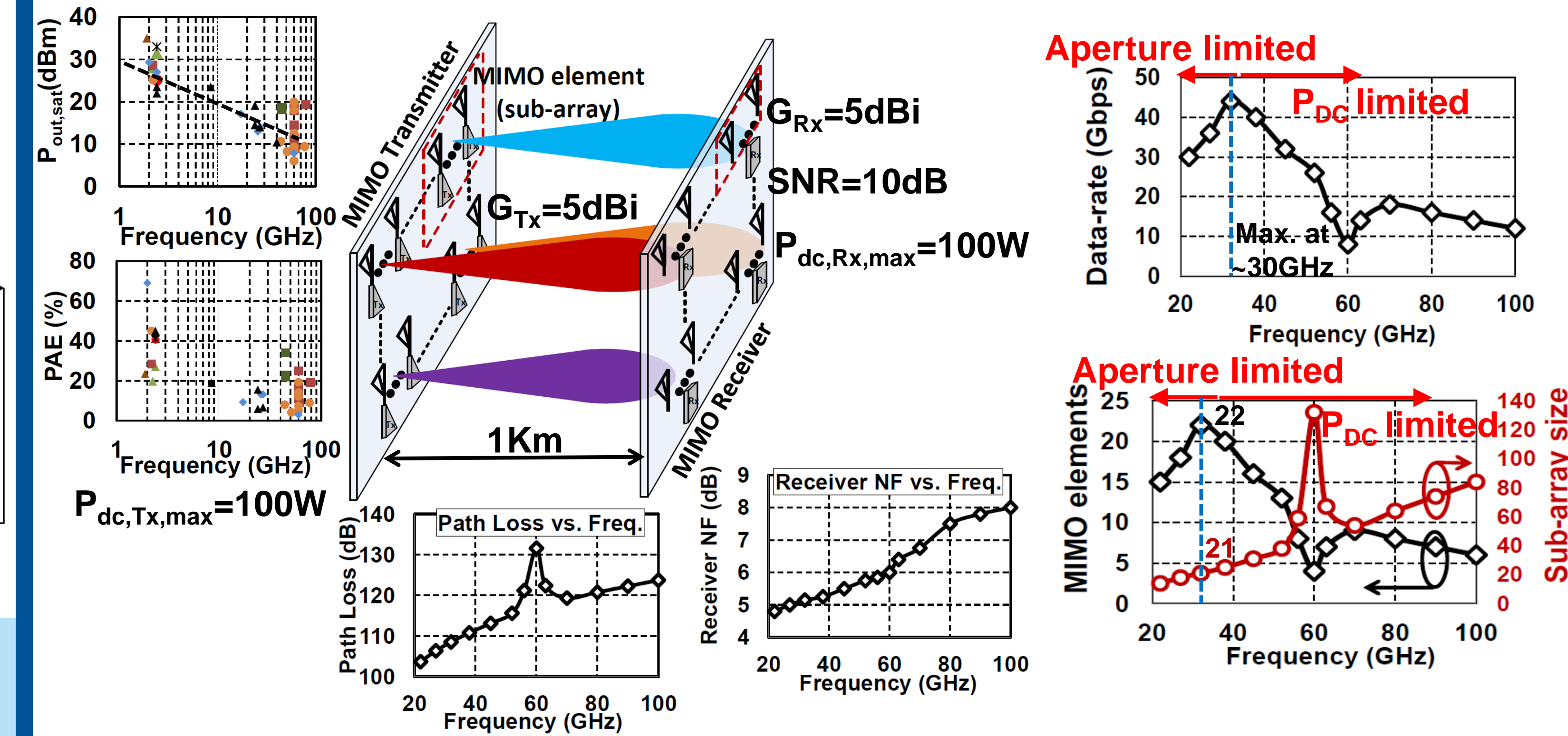- Difficult to scale to multicast.

The mmWave Spectrum

Feature-size

Wavelength (mm)

Attenuation (dB/Km)

Frequency (GHz) Bandwidth

Massive mmWave MIMO to replace fiber-optics for flexible high-data-rate backbone links.

Massive MIMO for Wireless Backhaul

MIMO Tx Sub-array Element

nV_{DD}

DAC Phase Decoder

Switched Cap. Supply Mod.

$2nV_{DD}$

$\phi[0:M-1]$

Freq. Mult. Phase Shifter Phase Mod.

$2V_{DD}$

DAC Amplitude Decoder

$A[0:N-1]$

Stacked Power DAC

High Power Massive MIMO Tx

Massive MIMO Rx

This Work

MIMO Rx Element (sub-array)

RF Front-end

1-bit ADC To Decoder

Level-triggered Sampler

Channel Estimation using Event-driven Sampling & Orthogonal Pilots [$p_1(t),..p_n(t)$]
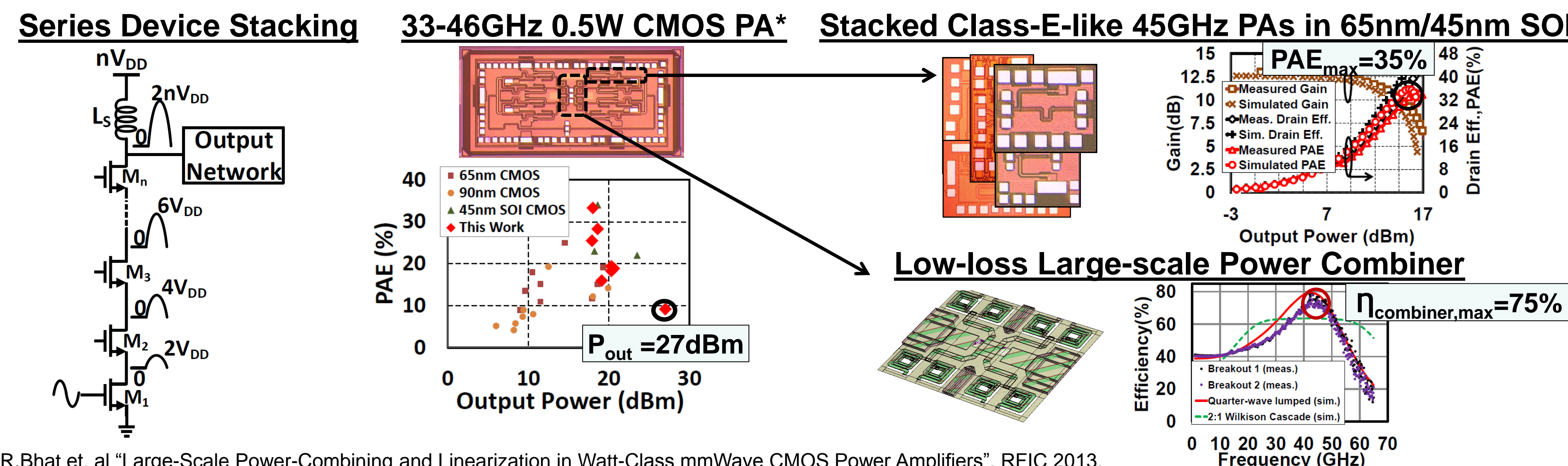
Reverse Link

$\hat{H}$

Massive MIMO requires novel mmWave Tx circuits and architectures with low-power TRx signal processing.

MIMO Data-rate: Fundamental Limits

$P_{out,sat}$ (dBm)

Frequency (GHz)

PAE (%)

Frequency (GHz)

$P_{dc,Tx,max}$=100W

Path Loss vs. Freq.

Path Loss (dB)

Frequency (GHz)

Receiver NF vs. Freq.

Receiver NF (dB)

Frequency (GHz)

MIMO Transmitter

MIMO element (sub-array)

G_{Rx}=5dBi

G_{Tx}=5dBi

SNR=10dB

$P_{dc,Rx,max}$=100W

1Km

MIMO Receiver

Aperture limited

P_{DC} limited

Data-rate (Gbps)

Max. at ~30GHz

Frequency (GHz)

Aperture limited

P_{DC} limited

MIMO elements

Sub-array size

Frequency (GHz)

High-power, Efficient mmWave "Digital" MIMO Tx

Prior Work: Stacked mmWave CMOS Watt-Class PAs

Series Device Stacking

nV_{DD}

$2nV_{DD}$

Output Network

$6V_{DD}$

$4V_{DD}$

$2V_{DD}$

M_n

M_3

M_2

M_1

33-46GHz 0.5W CMOS PA*

PAE (%)

- 65nm CMOS
- 90nm CMOS
- 45nm SOI CMOS
- This Work

P_{out} =27dBm

Output Power (dBm)

Stacked Class-E-like 45GHz PAs in 65nm/45nm SOI

PAE ≈35%

Gain (dB)

- Measured Gain
- Simulated Gain
- Meas. Drain Eff.
- Sim. Drain Eff.
- Measured PAE
- Simulated PAE

Output Power (dBm)

Drain Eff, PAE(%)

Low-loss Large-scale Power Combiner

$\eta_{combiner,max}$=75%

Efficiency(%)

- Breakout 1 (meas.)
- Breakout 2 (meas.)
- Quarter-wave lumped (sim.)
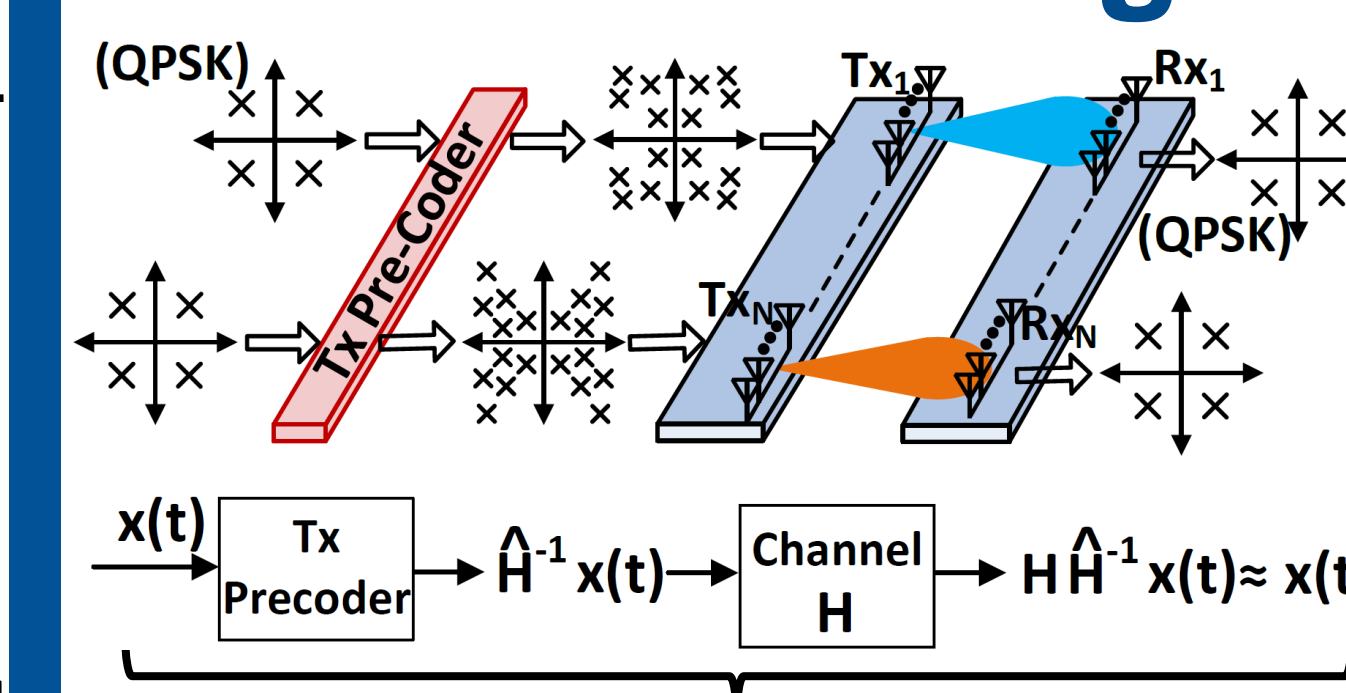- 2:1 Wilkison Cascade (sim.)

* R.Bhat et. al "Large-Scale Power-Combining and Linearization in Watt-Class mmWave CMOS Power Amplifiers", RFIC 2013.

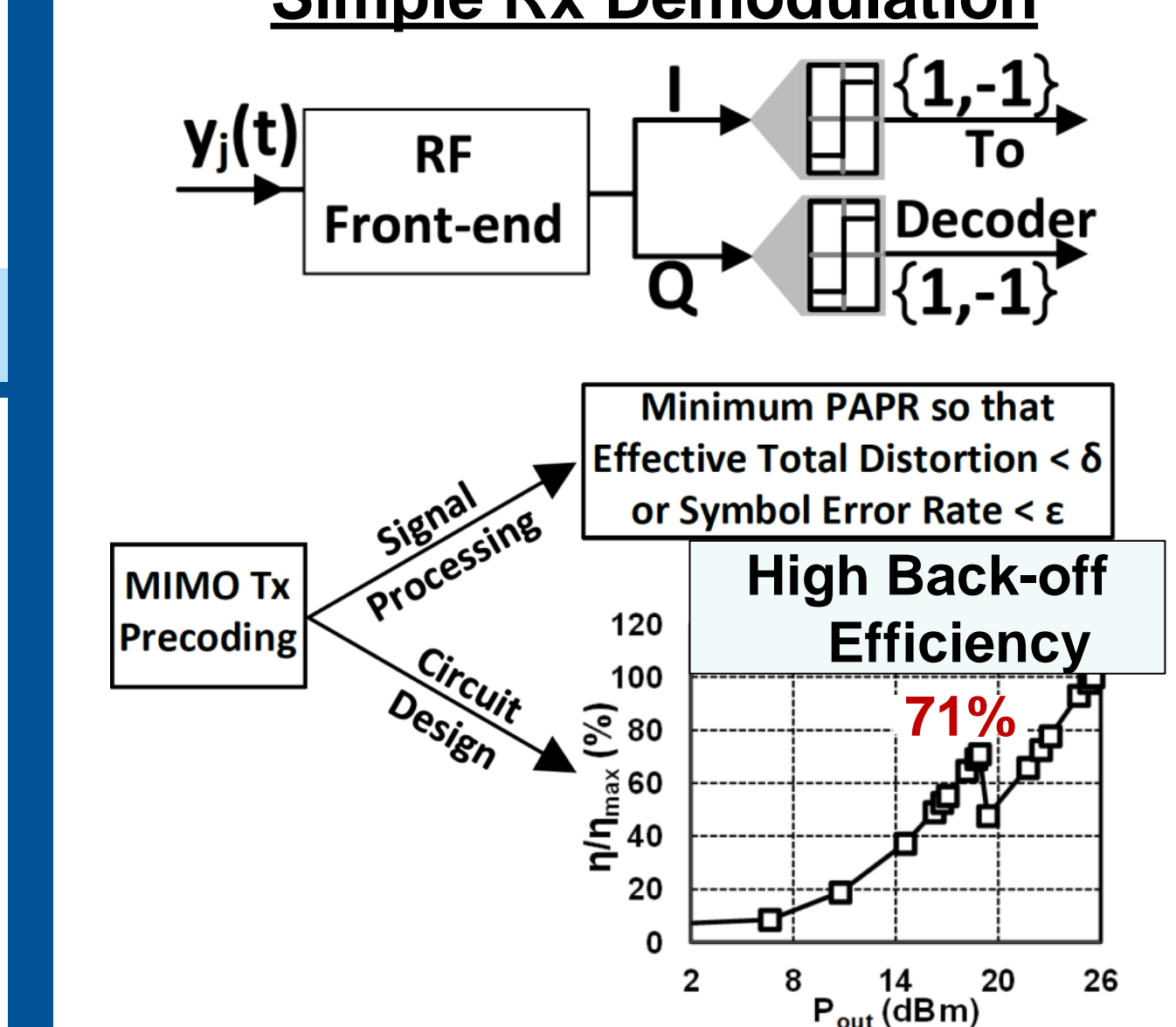**Stacking and large-scale power combining enable watt-class mmWave PAs.**

Proposed mmWave Digital Massive MIMO Tx
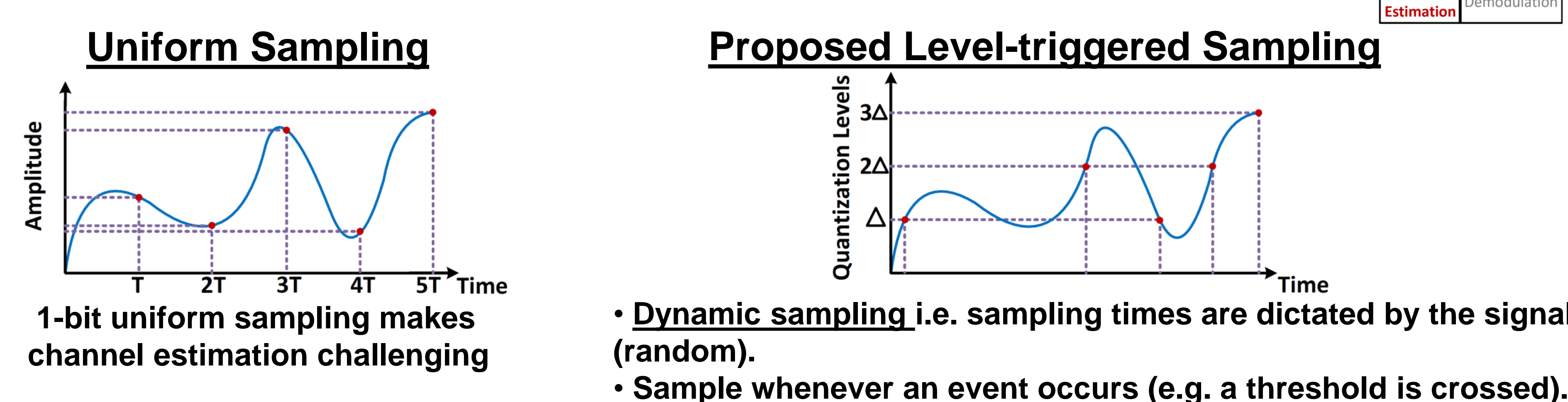
Massive MIMO Tx

MIMO element (sub-array)

Tx Pre-Coder

$V_{out} \alpha V_{DD,PA}$

Switched Cap. Supply Modulator Bank

$1:N_2$

$1:N_2$

$N_2:1$

$N_2:1$

V_{ref}

$V_{DD,PA}$

2stack Driver

Stacked Power DAC

A_N

A_{k-1}

Supply-adaptive Biasing

A_i

i=k,...N-1

$V_{DD,PA}$

M_4

M_3

M_2

M_1

V_{g4}

V_{g3}

V_{g2}

V_{g1}

V_{out}

V_{in}

- High-power Stacked Class-E-like Power DAC.
- Digital Polar Tx Architecture.
- Switched-capacitor Supply Modulation for Efficiency Under Back-off.
- Adaptive Biasing to Maintain Class-E Operation.
- Tail Transistor Switching for High Resolution.

Sub-array Element

MIMO Tx using stacked high-resolution mmWave power DACs with high back-off efficiency.

Supply Adaptive Biasing

4.8V

$V_{DD,PA}$(Variable)

R_{bias}

R_1

R_1

R_1

R_1

$V_3 = 3V_{DD,PA}/4$

$V_2 = V_{DD,PA}/2$

$V_1 = V_{DD,PA}/4$

I_{ref}

M_{1-3}

M_4

$M_{g,4}$

$M_{g,2}$

$M_{g,1}$

V_{out} (V)

V_{DD}(V)

- Voltage Div. Bias
- Adaptive Bias

Supply Impedance (Ω)

V_{DD}(V)

Drain Eff. (%)

P_{out}(dBm)

M_{1-3}=PMOS Level Shifters

$V_{g,1-4}$ =PA gate biases

$V_{g,i} = V_{g,1} + (i-1)V_{DD,PA}$

Adaptive biasing for stacked Class-E operation across supply voltages.

Hybrid mmWave Power DAC

1:2 (η=80%) (Switched Cap. converter)

2.4V

2stack Driver

4stack PA

$V_{DD,PA}$

V_{out}

1:1 (η=100%) (Supply-switch)

P_{sat}=25.5dBm

η_{-6dB}=0.71 ×η_{max}(33%)

2.4V

7 bit

Drain Eff. (%)

P_{out} (dBm)

- Hybrid Power DAC
- Tail Switched Power DAC

PAE (%)

P_{out} (dBm)

- Hybrid Power DAC
- Tail Switched Power DAC

V_{out} (V)

Amplitude Word

AM-PM (Degrees)

- Vout
- AM-PM

*Pre-layout results at 60GHz

High-resolution supply-modulated mmWave DAC with high $\eta_{back-off}$.

Cross-layer Aspects

Tx Precoding

(QPSK)

Tx_1

Rx_1

Tx Pre-Coder

Tx_{NT}

Rx_N

(QPSK)

$x(t)$

Tx Precoder

$\hat{H}^{-1}x(t)$

Channel H

$H\hat{H}^{-1}x(t) \approx x(t)$

Simple Rx Demodulation

$y_j(t)$

RF Front-end

I

Q

To Decoder

{1,-1}

{1,-1}

MIMO Tx Precoding

Signal Processing

Circuit Design

Minimum PAPR so that Effective Total Distortion < δ or Symbol Error Rate < ε

High Back-off Efficiency

71%

$\eta|_{max}$ (%)

P_{out} (dBm)

Co-design of low-PAPR precoding and Tx architecture with programmable back-off profile.

Level-triggered Signal Processing*

Analog Input

V_{ref}

V_{ref}

1-bit Level-triggered Sampling

Continuous-time DSP

* M. Kurchuk et al. "Event-Driven GHz-Range Continuous-Time Digital Signal Processor With Activity-Dependent Power Dissipation" IEEE JSSC, Sept. 2012.

Circuits for 1-bit level-triggered estimation is a topic for future research.

Event-driven Massive MIMO Channel Estimation

MIMO Channel Estimation

Pilots | Data
Channel Estimation | Demodulation

Uniform Sampling

Amplitude

T 2T 3T 4T 5T Time

Proposed Level-triggered Sampling

3Δ

2Δ

Δ

Quantization Levels

Time

- 1-bit uniform sampling makes channel estimation challenging

- Dynamic sampling i.e. sampling times are dictated by the signal (random).
- Sample whenever an event occurs (e.g. a threshold is crossed).

1-bit level-triggered sampling for channel estimation enables low-power massive MIMO Rx architecture.

Sequential Channel Estimator
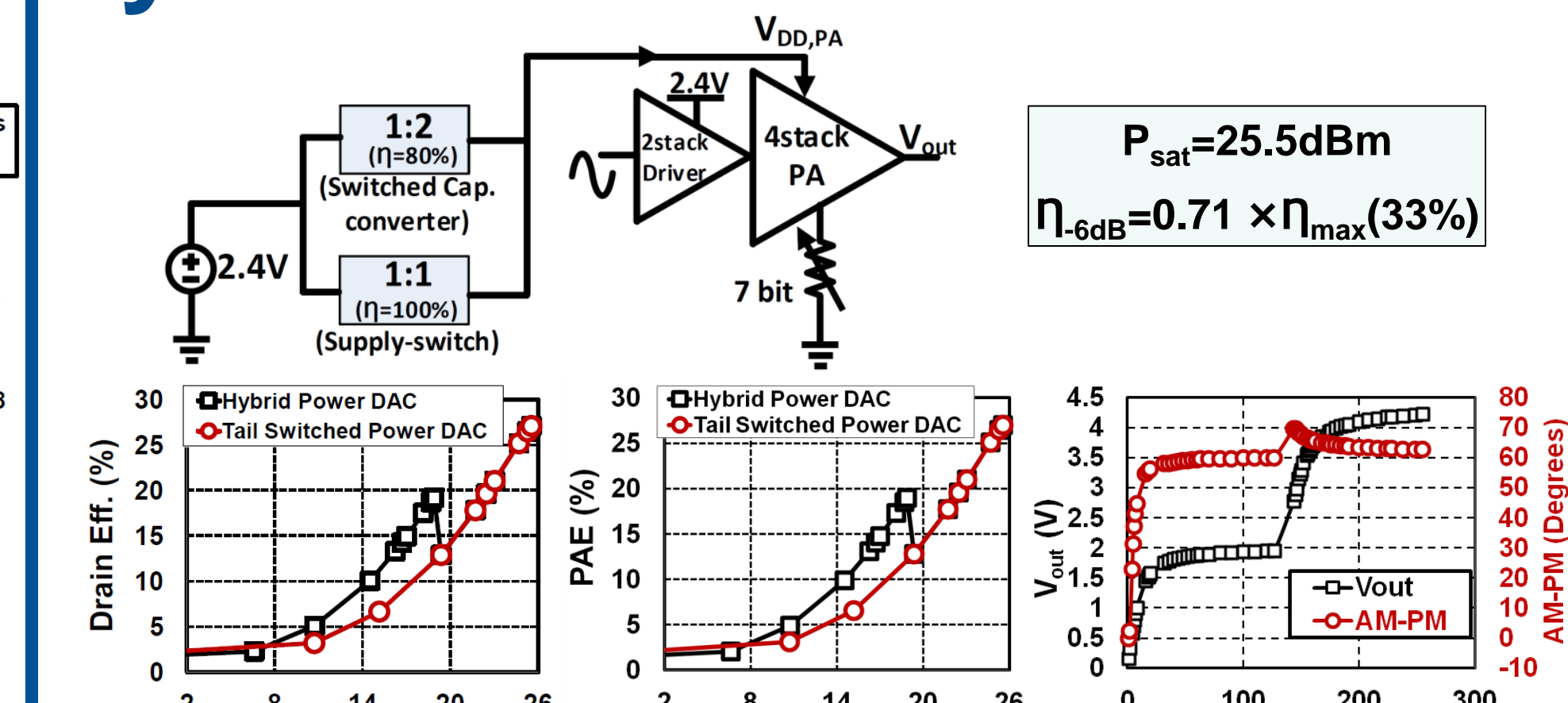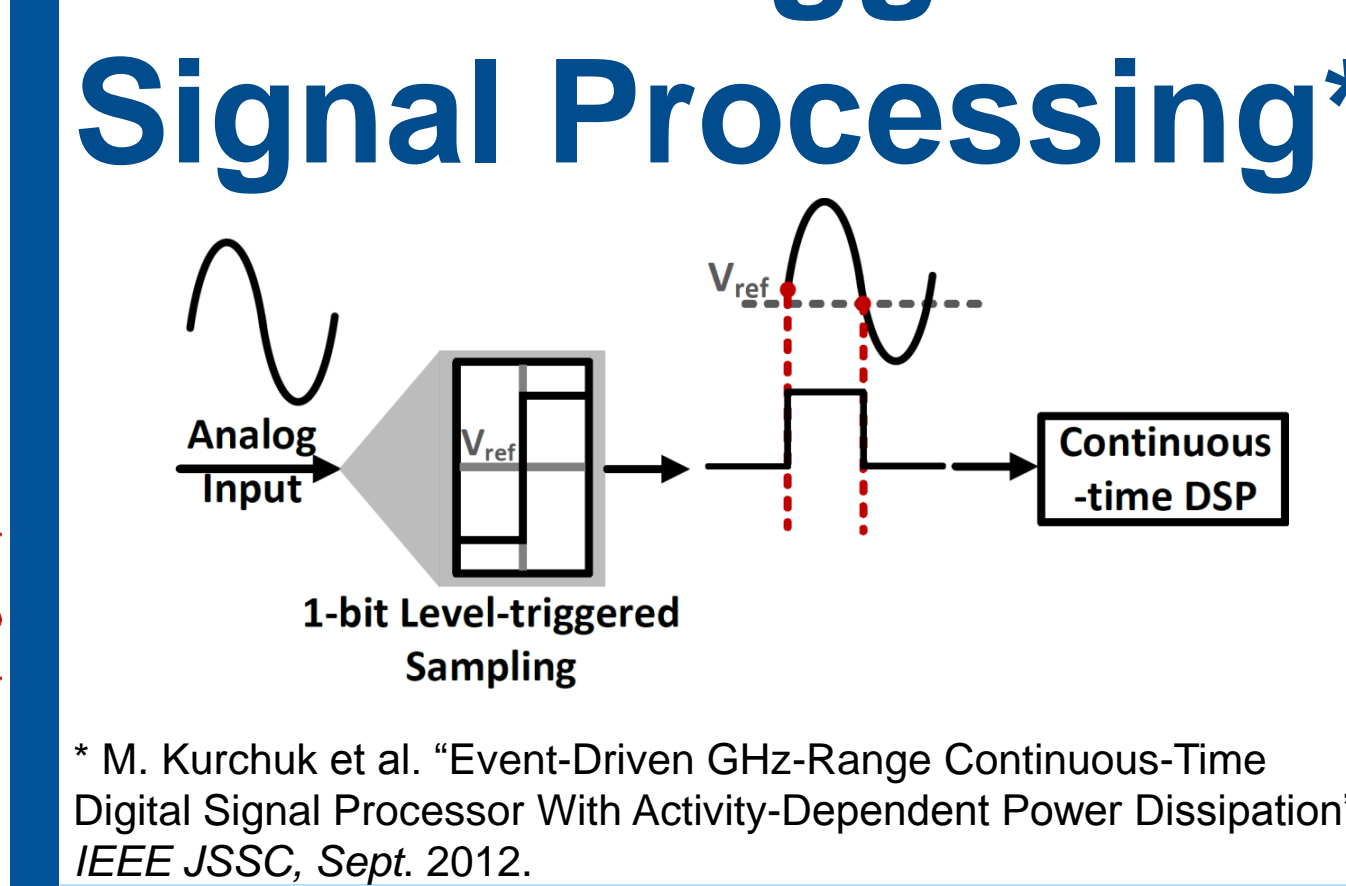
Pilots | Data
Channel Estimation | Demodulation

Analog Phase Inversion

$p_1(t)$

Level Triggered Sampler

$y_j(t)$

$p_2(t)$

$p_N(t)$

Channel Estimator

$\hat{h}_{1j}$

$\hat{h}_{ij}$

$\hat{h}_{Nj}$

$$\hat{h}_i = \frac{\int_{t=0}^{\tau_i} \frac{2Re\left((h_i^t)^* y_i^t\right)}{\sigma_i^2} dt}{\int_{t=0}^{\tau_i} \frac{2|h_i^t|^2}{\sigma_i^2} dt}$$

$$\tau_i = \frac{\mathcal{J}}{2|h_i|^2 \sigma_i^2}$$

- Exploits 1-bit sequence generated by level-triggered sampling.
- The approach lends itself to a low-power circuit implementation based on simple analog front-end processing.
- Asymptotically optimal sequential estimator with a novel sequential framework*.
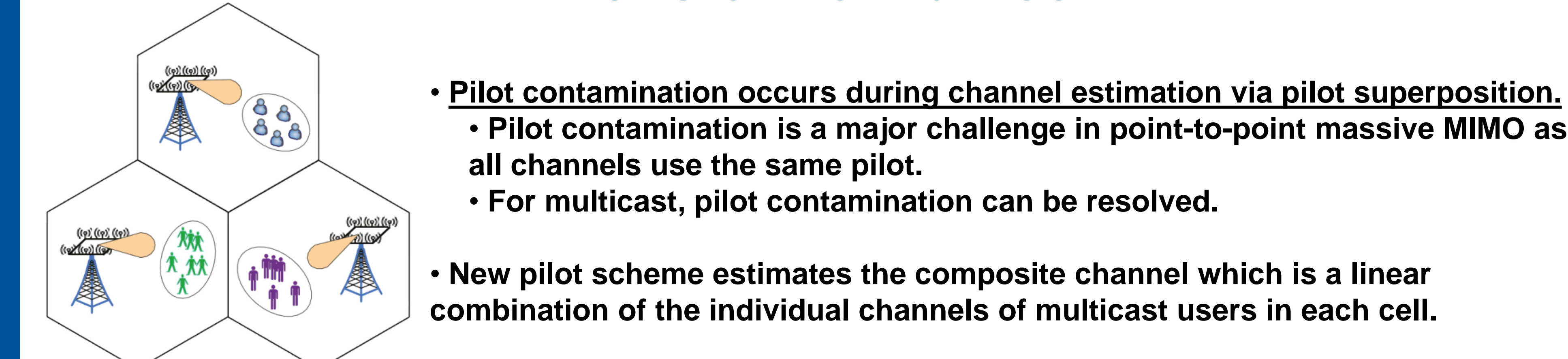- Benefits over fixed-time approach include higher estimation accuracy and availability of early estimates.

* Y. Yilmaz, and X. Wang "Sequential Decentralized Parameter Estimation under Randomly Observed Fisher Information" IT Trans, Feb. 2014.

Optimal sequential channel estimator exploits level-triggered sampling.

Extension to Multicell

Multicell Multicast Network

- Pilot contamination occurs during channel estimation via pilot superposition.
  - Pilot contamination is a major challenge in point-to-point massive MIMO as all channels use the same pilot.
  - For multicast, pilot contamination can be resolved.

- New pilot scheme estimates the composite channel which is a linear combination of the individual channels of multicast users in each cell.

New training scheme to resolve pilot contamination for multicast.