EE6312-SPRING 2012-Cadence Tutorial

January 28, 2012

Step 1

- Save the TSMC018_TEACHING.SCS model file, which you can find under http://www.ee.columbia.edu/ kinget/TOOLS/TSMC018_teaching.scs, into your directory tree as TSMC018_teaching.scs and use it in Artist → Set-up → Models. This file only has a model for the regular 1.8V devices for a typical (section tt), slow (section ss), and fast (section ff) process corner.
- Now create a Cadence directory for your files. You can name it "EE6312" for example, and create it with mkdir EE6312 at the prompt. Then change to that directory with cd EE6312.
- cd to the Cadence directory and run cadence with virtuoso &. The Virtuoso window is the main Cadence window, shown in Figure1 and also serves as the console where error messages appear.

Step 2

Once you have the Virtuoso window, click Tools → Library Manager to bring up the Library Manager. This is where all your designs are stored in a hierarchical

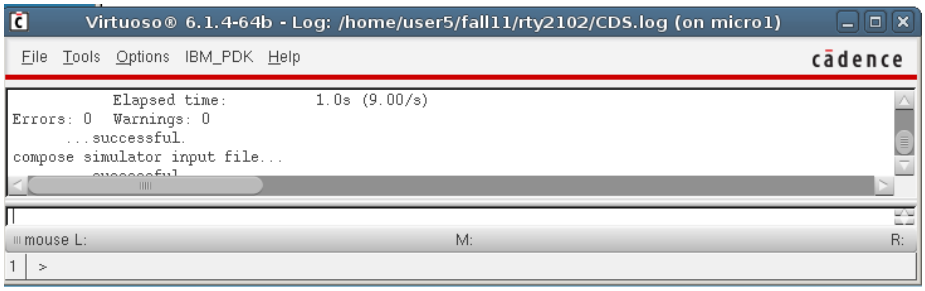

Figure 1: Virtuoso window

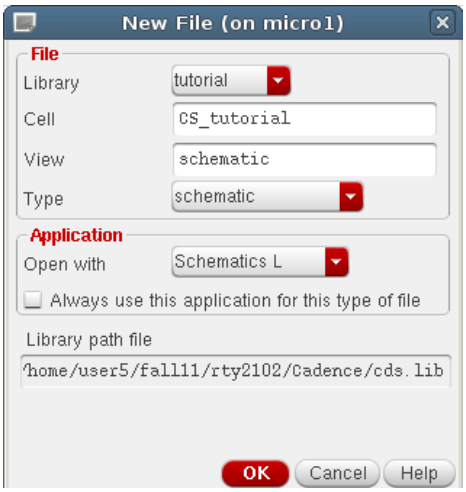

Figure 2: Create New File

fashion. To create a new project, go to File → New → Library.. and name it anything you want, for example tutorial. When it asks for a technology file, select "Don't need process information".

Step 3

The first thing we want to simulate is a CS amplifier as a tutorial example, so go again to File → New → Cell View.. and create a new Schematic view with cell name "CS_Tutorial" as shown in Figure2, and make sure it's in the tutorial library. Once you click OK, a new virtuoso schematic editing window should come up.

Step 4

Now we want to build a simple circuit to simulate, shown in Figure3. Cadence uses all three mouse buttons along many keyboard shortcuts. There is a contextual list of what each mouse button does at the bottom of the window. Let's put a MOSFET down first. Press i short for "instantiate" to bring up the instantiation dialog, shown in Figure4. If you remember the parameters of the part you want to use you can type it directly into the fields, otherwise browse for an "nmos4" symbol in the analogLib library as shown in Figure5. Note that the Instance window enlarges to show all the parameters associated with the item you have chosen to instantiate. Change the width to 10u M, the length to 0.18u M (10 μm/0.18 μm), multiplier to 1 and model name to "nch" leave everything else the same as shown in Figure6. Cadence accepts standard engi-

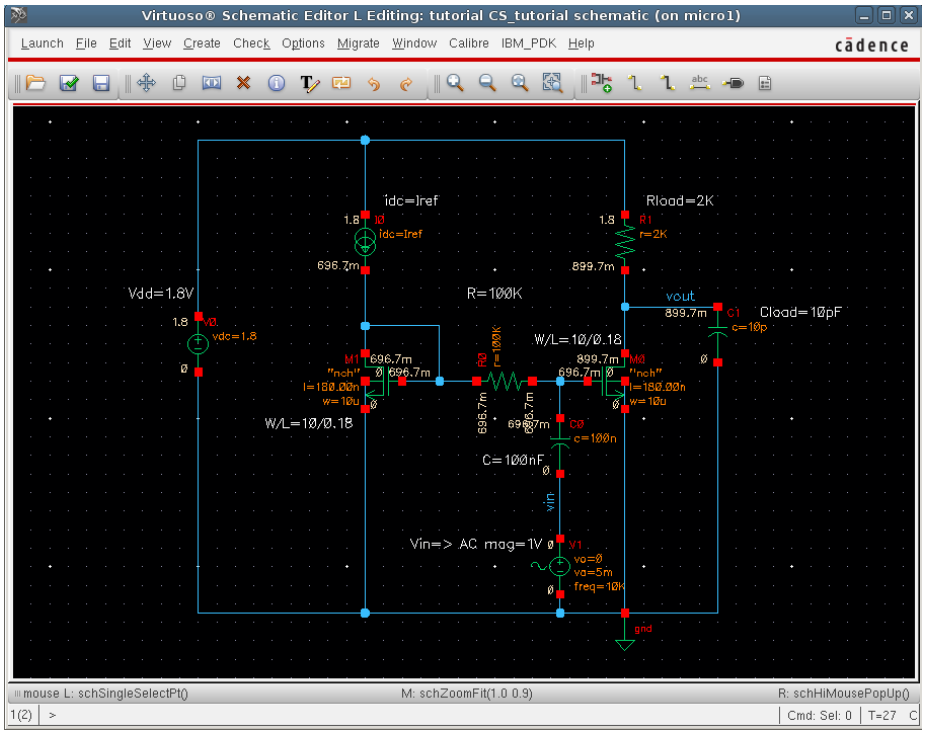

Figure 3: Schematic Window

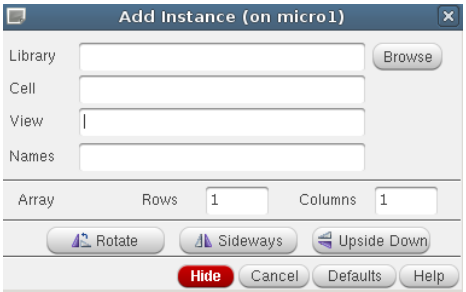

Figure 4: Add Instance

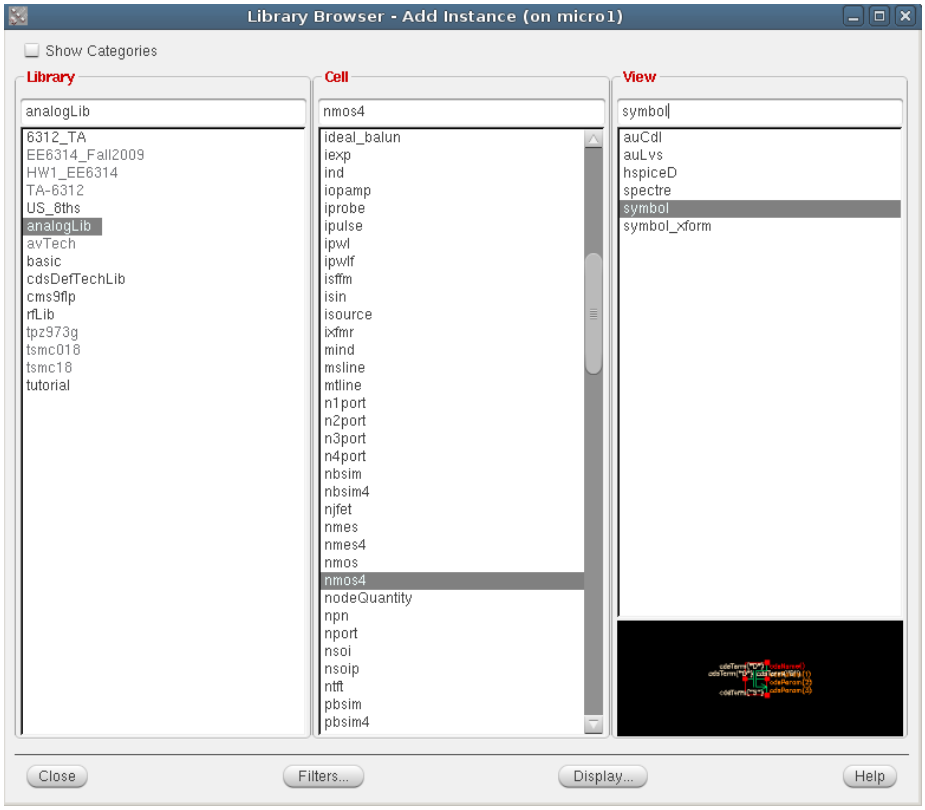

Figure 5: Library Browser

neering suffixes of units to simplify data entry.

Now when you bring the mouse back over the Virtuoso window, a MOSFET is being dragged. Left click to place it down.

Step 5

Items such as ideal passive elements, voltage and current sources and the like are all in the analogLib library.

- Instantiate a DC power source with a vdc cell set to a DC Voltage of 1.8V.
- Instantiate a DC current source with a idc cell set to a DC Current of "Iref" parameter for now.
- Instantiate an input voltage source vsin and set its parameters as shown, leaving all the others untouched for now as illustrated in Figure7.
- For the DC blocking cap and the load cap, use the ideal element cap in the analogLib, and set them to 100 nF and 10 pF, respectively.
- For the bias resistor and the load resistor, use the ideal resistor res also in the analogLib, with value 100 $k\Omega$ and 2 $k\Omega$, respectively.
- Now instantiate the Gnd symbol, which is called gnd, and only use one GND symbol in your toplevel (testbench) schematic so the simulator has a reference node.

If you want to view what you've done, f will fit the window to the full schematic, z will let you zoom into a selected region, and Shift-z will zoom out of a selected region.

Step 6

Now we want to wire it up. Press w to use the wire tool, and it's pretty easy. Cadence will try to snap to points that are attachable, or you can double-click to terminate a wire mid-route. Wire up the circuit, don't forget to wire up the substrate terminal of the MOSFET. When Cadence netlists the schematic to produce something to simulate, it will assign net names that aren't always readable. To specify wire names, press the l key (lowercase "L") to bring up the label dialog. List all the names you want to enter separated by a space, as illustrated in Figure8.

Avoid global names. Do not make any connections by naming. Use wires to connect nodes and elements. Now click the wires you'd like to label. To add notes, press the Shift-l key (lowercase "L") to bring up the note text dialog. Your schematic should now be done and look like Figure3.

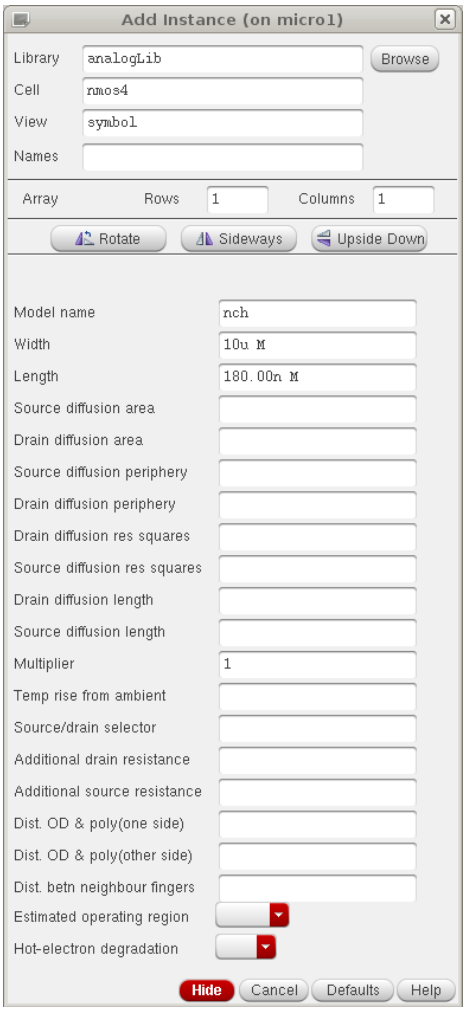

Figure 6: Edit Transistor Parameters

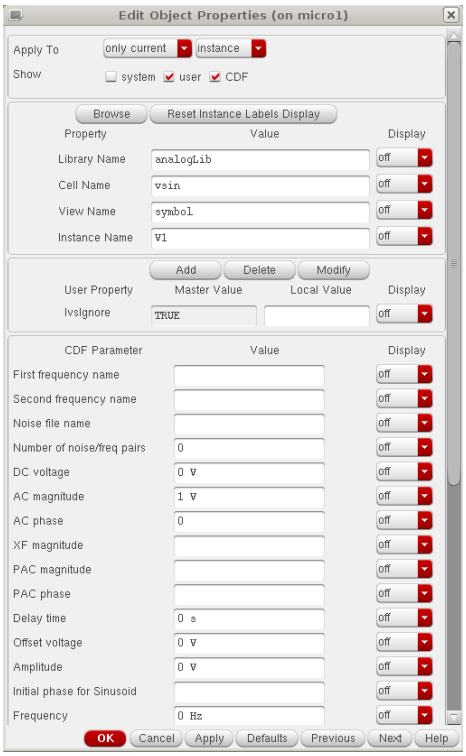

Figure 7: Edit Input Voltage Source vsin

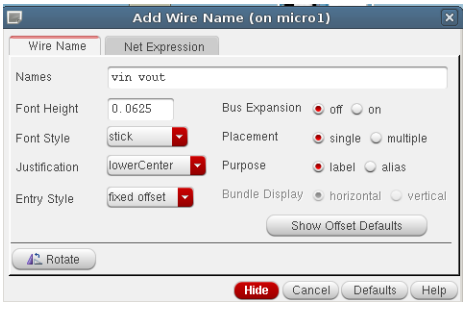

Figure 8: Add Wire Name

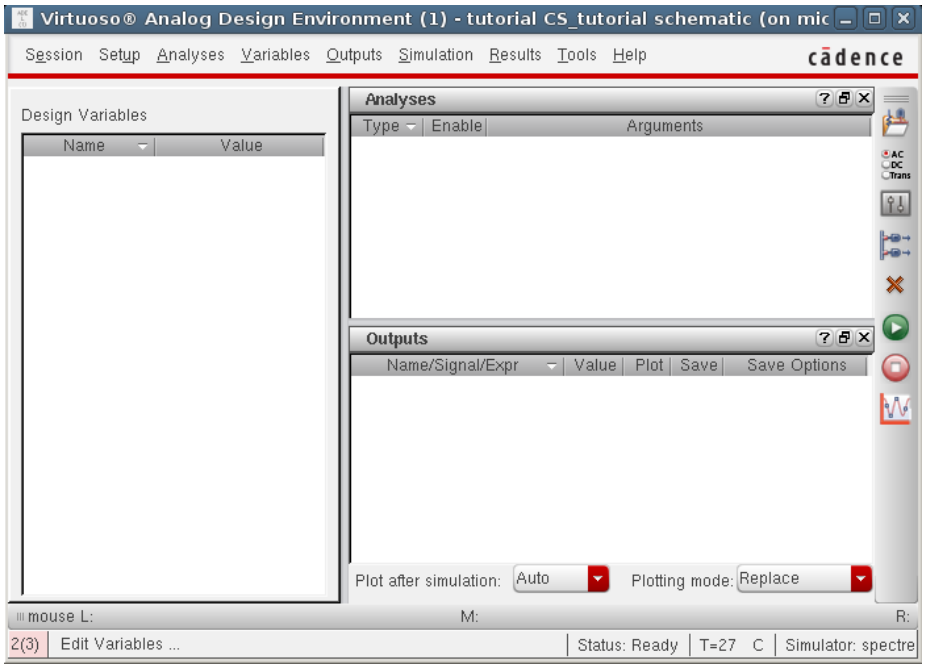

Figure 9: Analog Design Environment

Now click the checkbox right under File to check and save the schematic. If there are any errors or warnings, Cadence will tell you. An Error will for sure cause the simulation to not run, whereas a Warning is less severe and depending on the particular case is allowable. This schematic should return nothing, because it should have zero of each.

Step 7

Now we want to run a DC simulation. The DC analysis is used to find the DC operating point or DC transfer curves of the circuit. Go to Launch → ADE L to bring up the simulation window which is illustrated in Figure9. The first thing we need to do is specify the simulation engine and the directory for the simulation. Go to Setup → Simulator/Directory/Host... and choose the simulator spectre and the project directory /tmp. Once this finishes, we need to specify the model files for our devices. Do this by going to Setup → Model Libraries... and then add the following model library file: TSMC018_teaching.scs
Then specify "tt" for Section and later you will change it to "ff" and "ss" for corner cases. Then click OK to exit. Next we import the variables from the schematic. The easiest way to do this is have Cadence grab them from the schematic by going to Variables → Copy From Cellview which should cause Iref

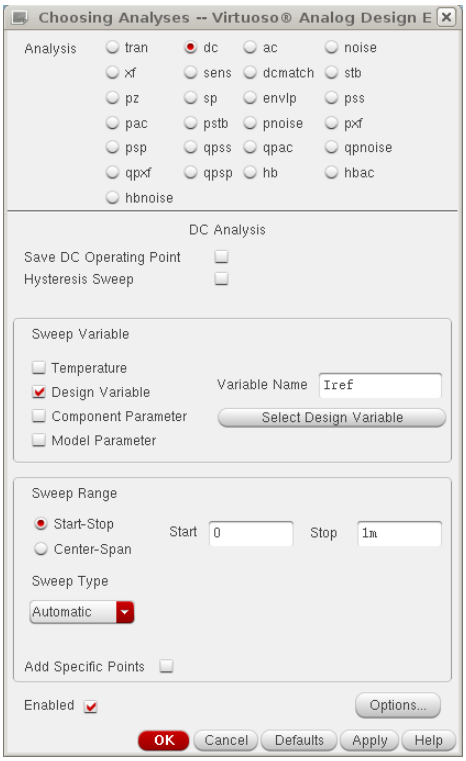

Figure 10: DC Sweep Analysis Setup

to appear in the lower left window. Cadence needs all variables initialized to some value (even if it is a sweep variable and will change) so double-click Iref, enter 0 for its value, click Change then OK to exit.

Step 8

Next go to Analyses → Choose to setup our DC sweep. Configure it as shown in Figure10. Now setup which variables you'd like to see plotted. There are again many ways to do this, but in the beginning it's easiest to just choose them on the schematic. Go to Outputs → To Be Plotted → Select On Schematic then click vout in the schematic window. It should highlight. Press ESC otherwise you will continue to select nets, which may not be desirable. The simulator window should look like Figure11.

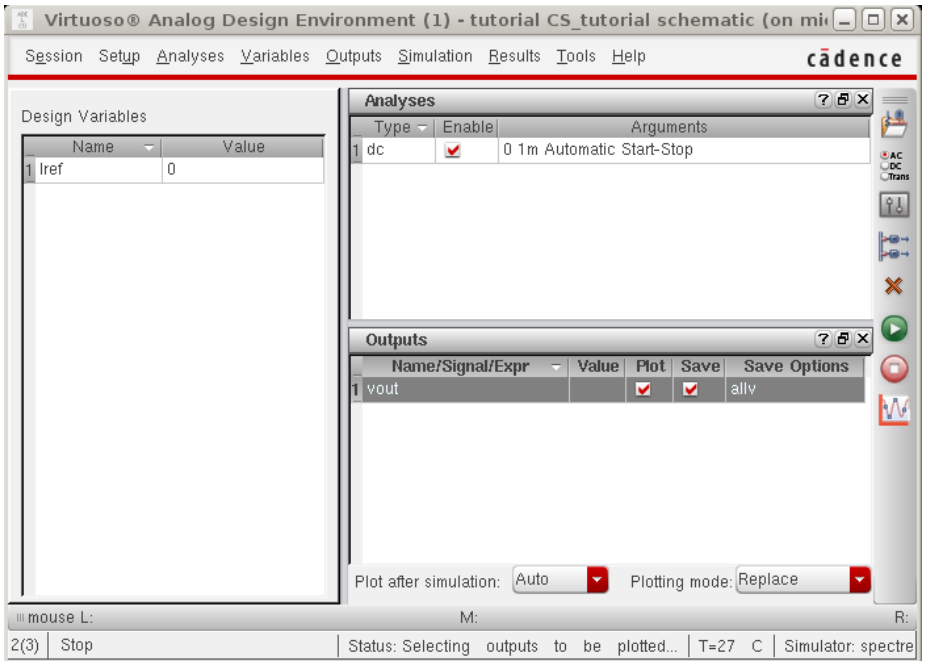

Figure 11: Analog Design Environment_1

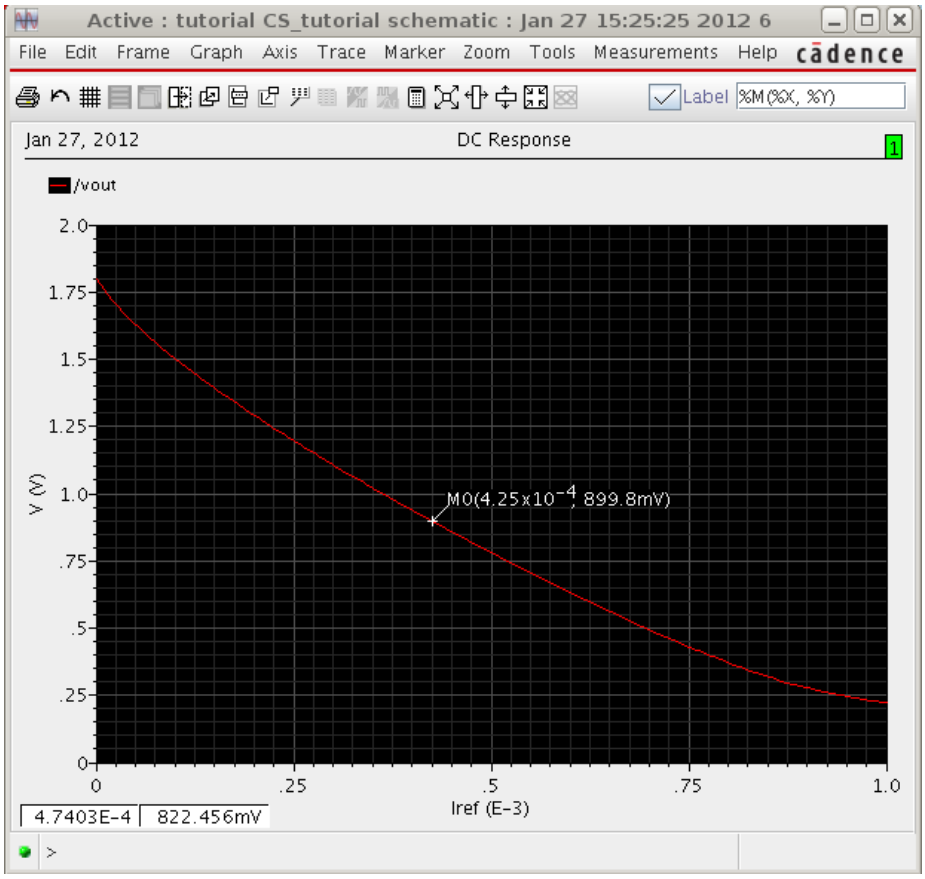

Figure 12: Vout (V) vs. Iref (mA)

Step 9

Now just click the third button from the bottom on the right, "Netlist and Run". A notification will pop up but just choose "Don't show again" and click OK, and spectre will run. You should get a plot window as shown in Figure12. I placed a marker where we should set Iref, around 0.425 μA to get a DC output voltage of 0.9 V which is the midpoint of V_{DD}. Once we've set the bias condition, we can do further analyses.

Step 10

Now we can analyze the AC performance of the amplifier. The AC analysis linearizes the circuit about the DC operating point and computes the response to a given small sinusoidal stimulus. Go back to the simulation window, and

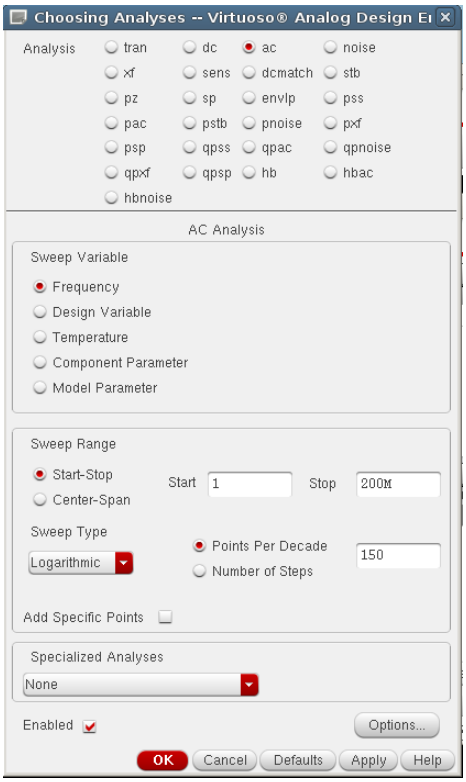

Figure 13: AC Analysis Setup

first update Iref to 0.425 μA, which will bias the transistor in saturation and strong inversion. Now go back to Analyses $\rightarrow$ Choose... and this time select ac analysis, and set it up like Figure13. Modify your DC analysis setup like Figure14. Run DC and AC analyses. Now let's look at the gain in dB, so we double-click the vout under Outputs of the simulator window, and change it to Figure15. The syntax of the calculator takes some getting used to. Netlisting and running this should produce the gain plot shown in Figure16. The midband gain is 14.83 dB.

Step 11

We can also do a transient analysis. Transient analysis computes the circuit solution as a function of time over a specified time range. From the gain plot, a frequency of 10kHz is in-band for the amplifier. So we can go back to our vsin source (in Virtuoso) and change it like Figure17. AC magnitude, AC phase, and DC voltage are for AC analysis, whereas Amplitude, Frequency and Delay time

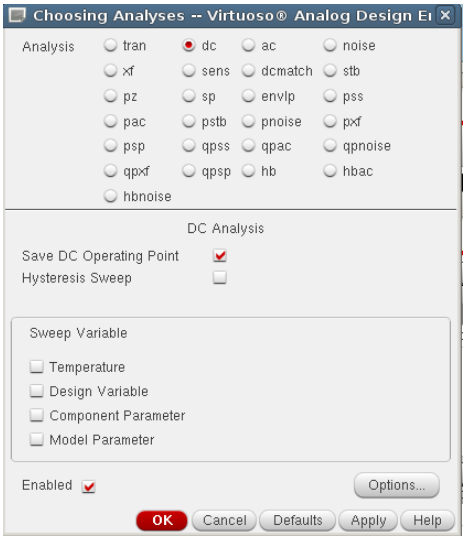

Figure 14: DC Analysis Setup

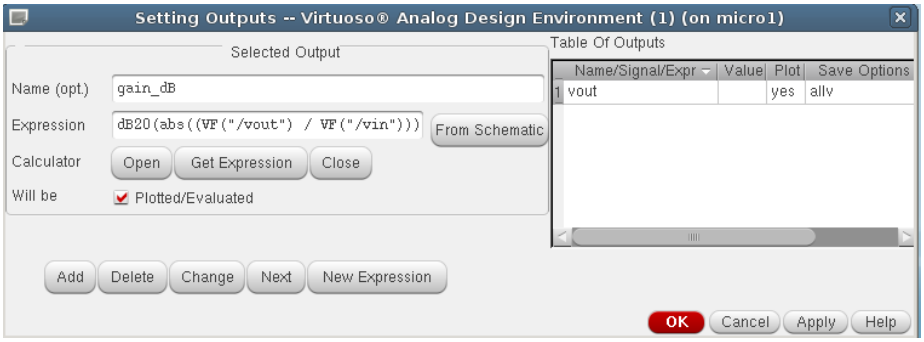

Figure 15: Set Gain Output

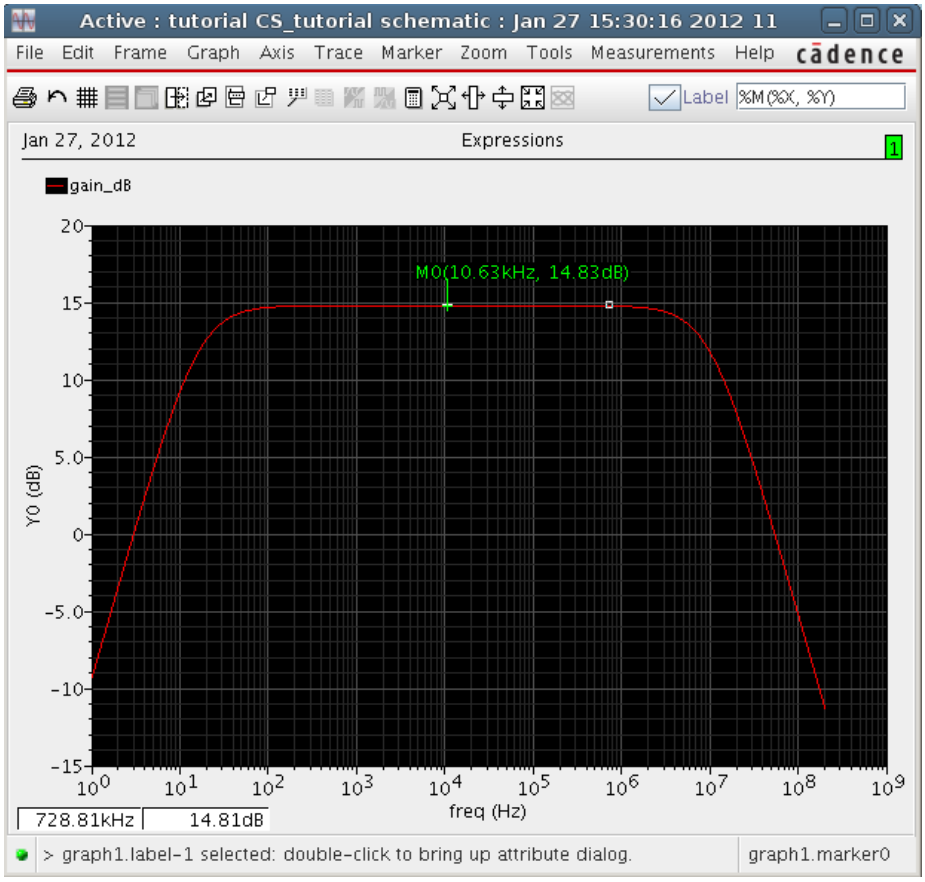

Figure 16: Gain (dB) vs. Frequency (Hz)

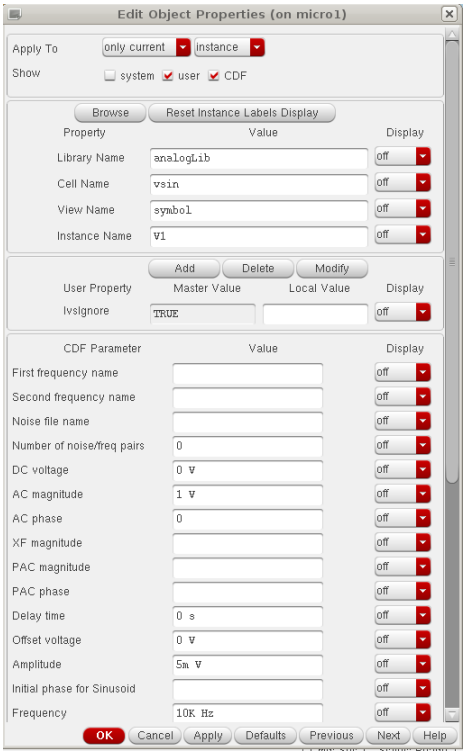

Figure 17: Edit Input Voltage Source vsin for Transient Analysis

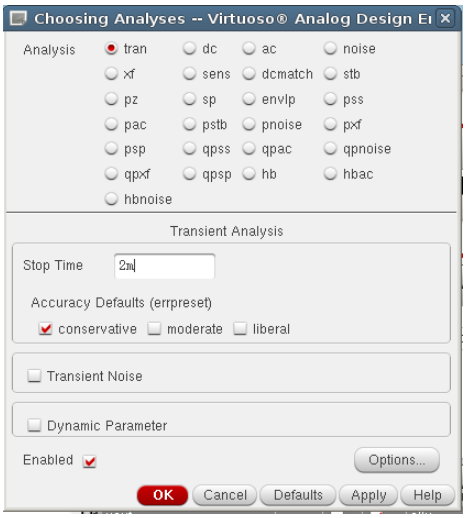

Figure 18: Transient Analysis Setup

are for transient analysis. For the transient analysis we need to ensure we're still operating in small-signal (for the purpose of this example, but you can simulate anything you'd like) so I chose a peak amplitude of 5mV. Check and save the schematic to be sure the simulator updates, otherwise when you try to run the netlist, you will get an unsuccessful warning in the virtuoso window. In the simulation setup, we now choose a transient analysis as illustrated in Figure18. We should also add back the input and output waves to the Outputs window, and deactivate the unneeded Analyses and Outputs. Double-click the AC analysis and in the lower-left corner de-select enabled so that only our DC and Tran analyses will run. The simulator should now look like Figure19. The simulation output is shown in Figure20. I have marked off the peak-peak output, which is 55 mV. The input peak-peak voltage is 10mV (5mV peak), so the gain magnitude is 5.5 V/V, which corresponds to the 14.83 dB seen in the AC analysis.

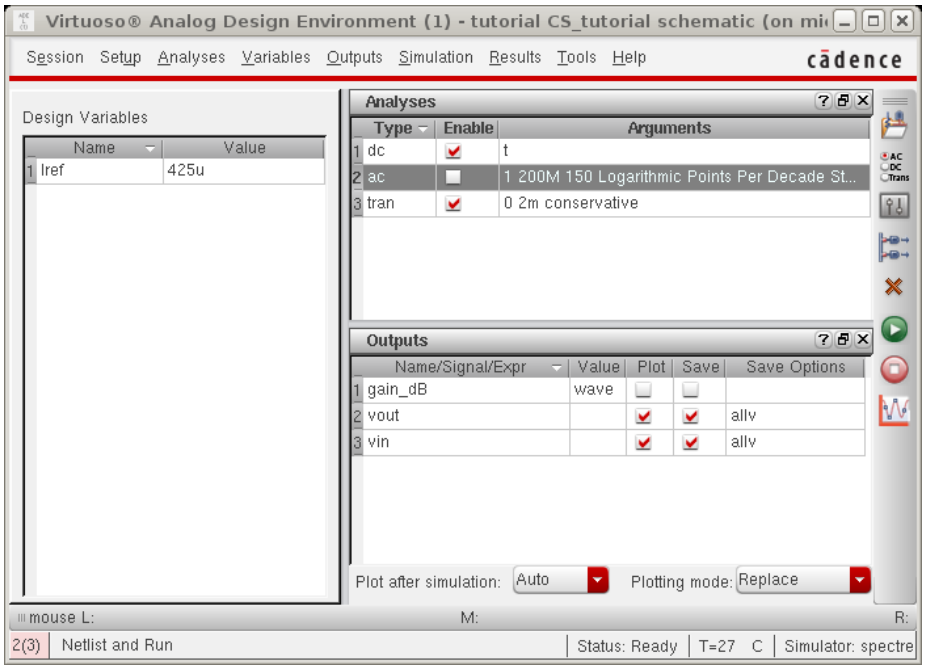

Figure 19: Analog Design Environment_2

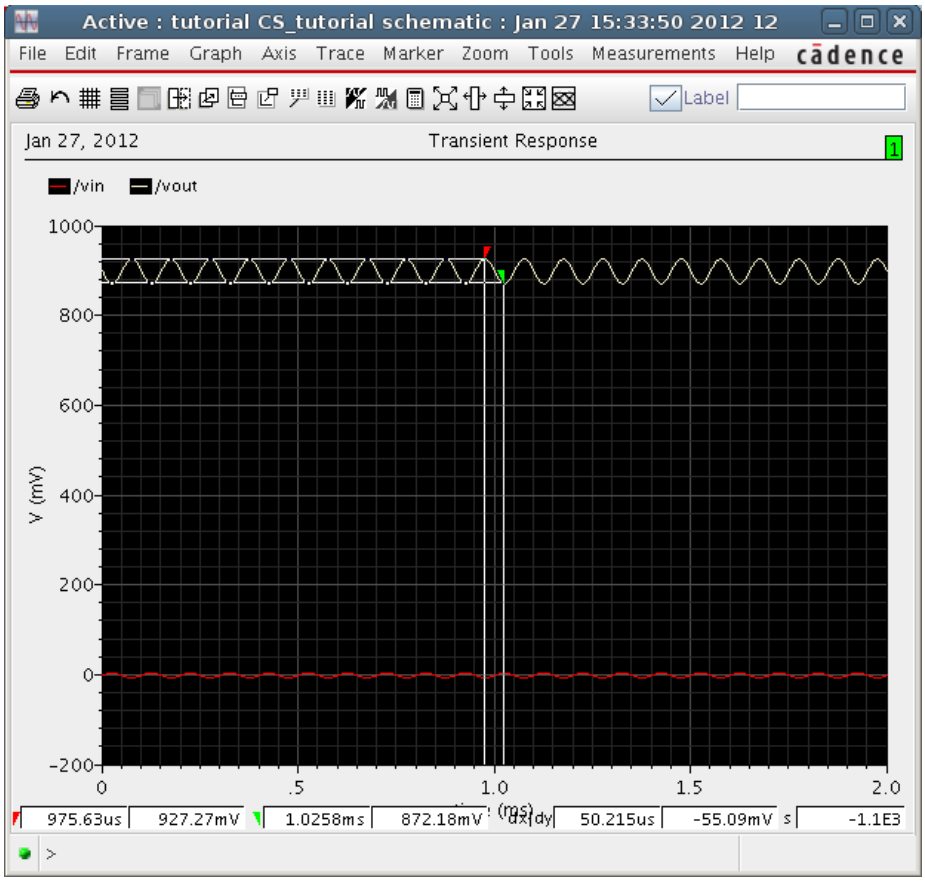

Figure 20: Vout (mV) vs. Time (ms) & Vin(mV) vs. Time (ms)