EE6312-SPRING 2012-Cadence Tutorial

January 28, 2012

Step 1

- Save the TSMC018_TEACHING.SCS model file, which you can find under http://www.ee.columbia.edu/ kinget/TOOLS/TSMC018_teaching.scs, into your directory tree as TSMC018_teaching.scs and use it in Artist → Setup → Models. This file only has a model for the regular 1.8V devices for a typical (section tt), slow (section ss), and fast (section ff) process corner.
- Now create a Cadence directory for your files. You can name it "EE6312" for example, and create it with mkdir EE6312 at the prompt. Then change to that directory with cd EE6312.
- cd to the Cadence directory and run cadence with virtuoso &. The Virtuoso window is the main Cadence window, shown in Figure 1 and also serves as the console where error messages appear.

Step 2

Once you have the Virtuoso window, click Tools \rightarrow Library Manager to bring up the Library Manager. This is where all your designs are stored in a hierarchical

C Virtuoso® 6.1.4-64b - L	.og: /home/user5/fall11/rty2102/CDS.log (on micro1)	_ - x
<u>File Tools Options IBM_PDK H</u> elp		cādence
Elapsed time: Errors: 0 Warnings: 0 successful. compose simulator input file	1.0s (9.00/s)	
 mouse L: 1 >	M:	R:

Figure 1: Virtuoso window



Figure 2: Create New File

fashion. To create a new project, go to File \rightarrow New \rightarrow Library.. and name it anything you want, for example tutorial. When it asks for a technology file, select "Don't need process information".

Step 3

The first thing we want to simulate is a CS amplifier as a tutorial example, so go again to File \rightarrow New \rightarrow Cell View.. and create a new Schematic view with cell name "CS_Tutorial" as shown in Figure2, and make sure it's in the tutorial library. Once you click OK, a new virtuoso schematic editing window should come up.

Step 4

Now we want to build a simple circuit to simulate, shown in Figure3. Cadence uses all three mouse buttons along many keyboard shortcuts. There is a contextual list of what each mouse button does at the bottom of the window. Let's put a MOSFET down first. Press i short for "instantiate" to bring up the instantiation dialog, shown in Figure4. If you remember the parameters of the part you want to use you can type it directly into the fields, otherwise browse for an "nmos4" symbol in the analogLib library as shown in Figure5. Note that the Instance window enlarges to show all the parameters associated with the item you have chosen to instantiate. Change the width to 10u M, the length to 0.18u M (10 μ m/0.18 μ m), multiplier to 1 and model name to "nch" leave everything else the same as shown in Figure6. Cadence accepts standard engi-



Figure 3: Schematic Window

	Add Instance (on micro1)
Library	Browse
Cell	
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Names	
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	Hide Cancel Defaults Help

Figure 4: Add Instance



Figure 5: Library Browser

neering suffixes of units to simplify data entry.

Now when you bring the mouse back over the Virtuoso window, a MOSFET is being dragged. Left click to place it down.

Step 5

Items such as ideal passive elements, voltage and current sources and the like are all in the analogLib library.

- Instantiate a DC power source with a vdc cell set to a DC Voltage of 1.8V.
- Instantiate a DC current source with a idc cell set to a DC Current of "Iref" parameter for now.
- Instantiate an input voltage source vsin and set its parameters as shown, leaving all the others untouched for now as illustrated in Figure 7.
- For the DC blocking cap and the load cap, use the ideal element cap in the analogLib, and set them to $100 \ nF$ and $10 \ pF$, respectively.
- For the bias resistor and the load resistor, use the ideal resistor res also in the analogLib, with value 100 $k\Omega$ and 2 $k\Omega$, respectively.
- Now instantiate the Gnd symbol, which is called gnd, and only use one GND symbol in your toplevel (testbench) schematic so the simulator has a reference node.

If you want to view what you've done, f will fit the window to the full schematic, z will let you zoom into a selected region, and Shift-z will zoom out of a selected region.

Step 6

Now we want to wire it up. Press w to use the wire tool, and it's pretty easy. Cadence will try to snap to points that are attachable, or you can double-click to terminate a wire mid-route. Wire up the circuit, don't forget to wire up the substrate terminal of the MOSFET. When Cadence netlists the schematic to produce something to simulate, it will assign net names that aren't always readable. To specify wire names, press the l key (lowercase "L") to bring up the label dialog. List all the names you want to enter separated by a space, as illustrated in Figure8.

Avoid global names. Do not make any connections by naming. Use wires to connect nodes and elements. Now click the wires you'd like to label. To add notes, press the Shift-l key (lowercase "L") to bring up the note text dialog. Your schematic should now be done and look like Figure3.

	Add Instan	ce (on micro1)	×
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Drain diffu	sion res squares		
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Source dit	fusion length		
Multiplier		1	
Temp rise	from ambient		
Source/dr	ain selector		
Additional	drain resistance		
Additional source resistance			
Dist. OD & poly(one side)			
Dist. OD & poly(other side)			
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Estimated operating region			
Hot-electron degradation			
	Hide	Cancel Defaults Hel	p

Figure 6: Edit Transistor Parameters

Apply To only curren	it 🔽 instance 🔽	
Show 🗌 system	🗹 user 🗹 CDF	
Browse	Reset Instance Labels Display	
Property	Value	Display
Library Name a	nalogLib	off
Cell Name 🗸	sin	off
View Name s	ymbol	off
Instance Name	1	off
(Add Delete Modify)
User Property	Master Value Local Value	Display
Ivsignore T	RUE	off
CDF Parameter	Value	Display
First frequency name		off
Second frequency name		off
Noise file name		off
Number of noise/freq pairs	0	off
DC voltage	0 4	off
AC magnitude	1 V	off
AC phase	0	off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Delay time	0 s	off
Offset voltage	0 ¥	off
Amplitude	0 ¥	off
Initial phase for Sinusoid off		off
Frequency	0 Hz	off

Figure 7: Edit Input Voltage Source vsin

	Add Wire N	ame (on micr	o1)	×
Wire Name	Net Expression			
Names	vin vout]
Font Height	0.0625	Bus Expansion	🖲 off 🔾 on	
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Justification	lowerCenter	Purpose	🖲 label 🔾 alias	
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		Sh	ow Offset Defaults	
🔼 Rotate				
		Hide Ca	ncel Defaults Help	5

Figure 8: Add Wire Name



Figure 9: Analog Design Environment

Now click the checkbox right under File to check and save the schematic. If there are any errors or warnings, Cadence will tell you. An Error will for sure cause the simulation to not run, whereas a Warning is less severe and depending on the particular case is allowable. This schematic should return nothing, because it should have zero of each.

Step 7

Now we want to run a DC simulation. The DC analysis is used to find the DC operating point or DC transfer curves of the circuit. Go to Launch \rightarrow ADE L to bring up the simulation window which is illustrated in Figure9. The first thing we need to do is specify the simulation engine and the directory for the simulation. Go to Setup \rightarrow Simulator/Directory/Host... and choose the simulator spectre and the project directory /tmp. Once this finishes, we need to specify the model files for our devices. Do this by going to Setup \rightarrow Model Libraries... and then add the following model library file: TSMC018_teaching.scs Then specify "tt" for Section and later you will change it to "ff" and "ss" for

corner cases. Then click OK to exit. Next we import the variables from the schematic. The easiest way to do this is have Cadence grab them from the schematic by going to Variables \rightarrow Copy From Cellview which should cause Iref

, Choosi	ng Analys	ses Vir	tuoso® A	nalog Design E
Analysis	🔾 tran	🖲 dc	🔾 ac	🔾 noise
	🔾 xf	🔾 sens	🔾 dcmatch	i 🔾 stb
	🔾 pz	🔾 sp	🔾 envlp	🔾 pss
	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise
	🔾 qp×f	🔾 dbsb	🔾 hb	🔾 hbac
	🔾 hbnois	e		
		DC An	alysis	
Save DC C	perating Poi	nt 📃		
Hysteresis	Sweep			
Sweep Va	ariable			
🔲 Tempe	rature			
✓ Design Variable Variable Name Iref				
Component Parameter Select Design Variable				
📃 Model	Parameter			
Sweep Ra	ange			
🖲 Start-S	Stop	Start 0		Ston 1m
🔾 Center	r-Span	0		210
Sweep Ty	pe			
Automatic				
Add Specif	îc Points 🗌			
Enabled 🛓	2			Options

Figure 10: DC Sweep Analysis Setup

to appear in the lower left window. Cadence needs all variables initialized to some value (even if it is a sweep variable and will change) so double-click Iref, enter 0 for its value, click Change then OK to exit.

Step 8

Next go to Analyses \rightarrow Choose to setup our DC sweep. Configure it as shown in Figure10. Now setup which variables you'd like to see plotted. There are again many ways to do this, but in the beginning it's easiest to just choose them on the schematic. Go to Outputs \rightarrow To Be Plotted \rightarrow Select On Schematic then click vout in the schematic window. It should highlight. Press ESC otherwise you will continue to select nets, which may not be desirable. The simulator window should look like Figure11.



Figure 11: Analog Design Environment_1



Figure 12: Vout (V) vs. Iref (mA)

Step 9

Now just click the third button from the bottom on the right, "Netlist and Run". A notification will pop up but just choose "Don't show again" and click OK, and spectre will run. You should get a plot window as shown in Figure 12. I placed a marker where we should set Iref, around 0.425 μA to get a DC output voltage of 0.9 V which is the midpoint of V_{DD} . Once we've set the bias condition, we can do further analyses.

Step 10

Now we can analyze the AC performance of the amplifier. The AC analysis linearizes the circuit about the DC operating point and computes the response to a given small sinusoidal stimulus. Go back to the simulation window, and

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Analysis	🔾 tran	🔾 dc	🖲 ac	🔾 noise	
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	🔾 pz	🔾 sp	🔾 envip	🔾 pss	
	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf	
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise	
	🔾 qpxf	🔾 dbsb	🔾 hb	🔾 hbac	
	🔾 hbnois	e			
		AC Ana	alysis		
Sweep Va	ariable				
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🔾 Model	l Parameter				
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Figure 13: AC Analysis Setup

first update Iref to 0.425 μA , which will bias the transistor in saturation and strong inversion. Now go back to Analyses \rightarrow Choose... and this time select ac analysis, and set it up like Figure13. Modify your DC analysis setup like Figure14. Run DC and AC analyses. Now let's look at the gain in dB, so we double-click the vout under Outputs of the simulator window, and change it to Figure15. The syntax of the calculator takes some getting used to. Netlisting and running this should produce the gain plot shown in Figure16. The midband gain is 14.83 dB.

Step 11

We can also do a transient analysis. Transient analysis computes the circuit solution as a function of time over a specified time range. From the gain plot, a frequency of 10kHz is in-band for the amplifier. So we can go back to our vsin source (in Virtuoso) and change it like Figure 17. AC magnitude, AC phase, and DC voltage are for AC analysis, whereas Amplitude, Frequency and Delay time

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Analysis	🔾 tran	🖲 dc	🔾 ac	🔾 noise	
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	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf	
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise	
	🔾 qpxf	🔾 qpsp	🔾 hb	🔾 hbac	
	🔾 hbnois	е			
		DC Ana	lysis		
Save DC C	perating Poi	int 🗹			
Hysteresis	Sweep				
Sweep Variable					
Townersture					
E Tempe	rature Mariable				
E Design	Design Variable				
	Faranleter				
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	0	Canc	el Default	ts Apply Help	

Figure 14: DC Analysis Setup

	Setting Outputs Virtuoso® Analog Design E	nvironment (1) (on micro1)
c ———	Selected Output	Table Of Outputs
	, , ,	Name/Signal/Expr - Value Plot Save Options
Name (opt.)	gain_dB	1 vout yes allv
Expression	dB20(abs((VF("/vout") / VF("/vin")))) From Schematic	
Calculator	Open Get Expression Close	
Will be	✓ Plotted/Evaluated	
Add	Delete Change Next New Expression	
		OK Cancel Apply Help

Figure 15: Set Gain Output



Figure 16: Gain (dB) vs. Frequency (Hz)

Apply To only curre	ent 🔽 instance 🔽	
Show 🔄 system	🗹 user 🗹 CDF	
Browse	Reset Instance Labels Display	
Property	Value	Display
Library Name	analogLib	off 🔽
Cell Name	vsin	off 🔽
View Name	symbol	off 🔽
Instance Name	¥1	off 🔽
(Add Delete Modify)
User Property	Master Value Local Value	Display
Ivsignore	TRUE	off 🔽
CDF Parameter	Value	Display
First frequency name		off 🔽
Second frequency name		off 🔽
Noise file name		off 🔽
Number of noise/freq pairs	0	off 🔽
DC voltage	0 4	off 🔽
AC magnitude	1 V	off 🔽
AC phase	0	off 🔽
XF magnitude		off 🔽
PAC magnitude		off 🔽
PAC phase		off 🔽
Delay time	0 s	off 🔽
Offset voltage	0 4	off 🔽
Amplitude	5m V	off 🔽
Initial phase for Sinusoid		off 🔽
Frequency	10K Hz	off 🔽

Figure 17: Edit Input Voltage Source vsin for Transient Analysis

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Analysis	🖲 tran	🔾 dc	🔾 ac	🔾 noise
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	🔾 pz	🔾 sp	🔾 envlp	🔾 pss
	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise
	🔾 qpxf	🔾 qpsp	🔾 hb	🔾 hbac
	🔾 hbnoise	e		
Transient Analysis				
Stop Time 2ml				
Accuracy Defaults (errpreset)				
🗹 conservative 📃 moderate 🛄 liberal				
Transient Noise				
Dynamic Parameter				
Enabled 🖌 Options				
OK Cancel Defaults Apply Help				

Figure 18: Transient Analysis Setup

are for transient analysis. For the transient analysis we need to ensure we're still operating in small-signal (for the purpose of this example, but you can simulate anything you'd like) so I chose a peak amplitude of 5mV. Check and save the schematic to be sure the simulator updates, otherwise when you try to run the netlist, you will get an unsuccessful warning in the virtuoso window. In the simulation setup, we now choose a transient analysis as illustrated in Figure18. We should also add back the input and output waves to the Outputs window, and deactivate the unneeded Analyses and Outputs. Double-click the AC analysis and in the lower-left corner de-select enabled so that only our DC and Tran analyses will run. The simulator should now look like Figure19. The simulation output is shown in Figure20. I have marked off the peak-peak output, which is 55 mV. The input peak-peak voltage is 10mV (5mV peak), so the gain magnitude is 5.5 V/V, which corresponds to the 14.83 dB seen in the AC analysis.

📲 Virtuoso® Analog Design Environment (1) - tutorial CS_tutorial schematic (on mic 🗐 🗖 🗷			
S <u>e</u> ssion Set <u>u</u> p <u>A</u> nalyses <u>V</u> ariables <u>C</u>	outputs <u>Simulation Results Tools H</u> elp cādence		
Design Variables Name Value 1 Iref 425u	Analyses ? × Type ~ Enable Arguments 1 dc ✓ t 2 ac 1 200M 150 Logarithmic Points Per Decade St Accession 3 tran ✓ 0 2m conservative *** X X		
	Outputs Image: Constraint of the second se		
mmouse L:	Plot after simulation: Auto Plotting mode: Replace R: R:		
2(3) Netlist and Run	Status: Ready T=27 C Simulator: spectre		

Figure 19: Analog Design Environment_2



Figure 20: Vout (mV) vs. Time (ms) & Vin(mV) vs. Time (ms)