CAD 5 – DATA PATH

EE 477

Yexuan Chen, Yuxiang Chen, Xinyi Chang

1. Introduction:

The purpose of this project is to assemble the data path for our baseline microprocessor. The datapath of our baseline microprocessor is made up of the register file, the shifter, the ALU, the zero detect module and a selection Mux.

2. Analytical Approach

Based on the verilog model provided, we connected all the required path together, which includes a ALU, a shifter, a register file, a zero-detector and a selection mux. In order to make the layout easy to connect and have an appropriate layout ratio, we stacked all the components from top to bottom so that the metal tracks can go vertically as direct as possible. It will not only avoid unnecessary routing, but also improve post-layout performance.

3. Schematic

Figure 3.3 shows the schematic design of the data path. Figure 3.1 and Figure 3.2 shows the zero-detector module and the selection Mux in detail. All other parts of data path are same as previous projects. All the simulation waveforms is placed in the “verification” section.

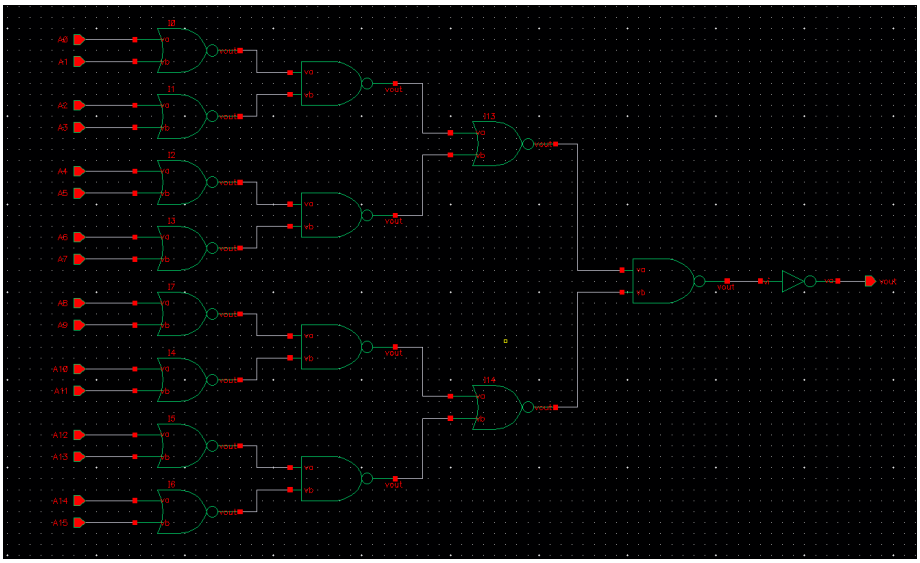

Figure 3.2 Schematic Design of the Zero-detector module

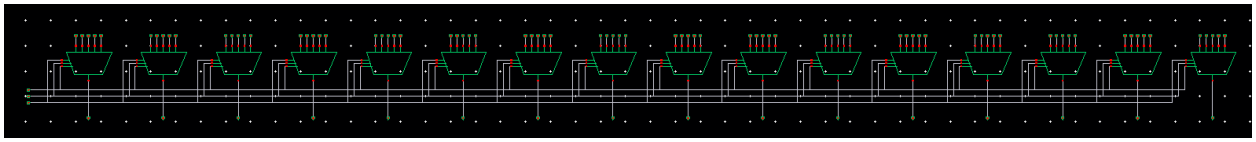

Figure 3.2 Schematic Design of Selection Mux

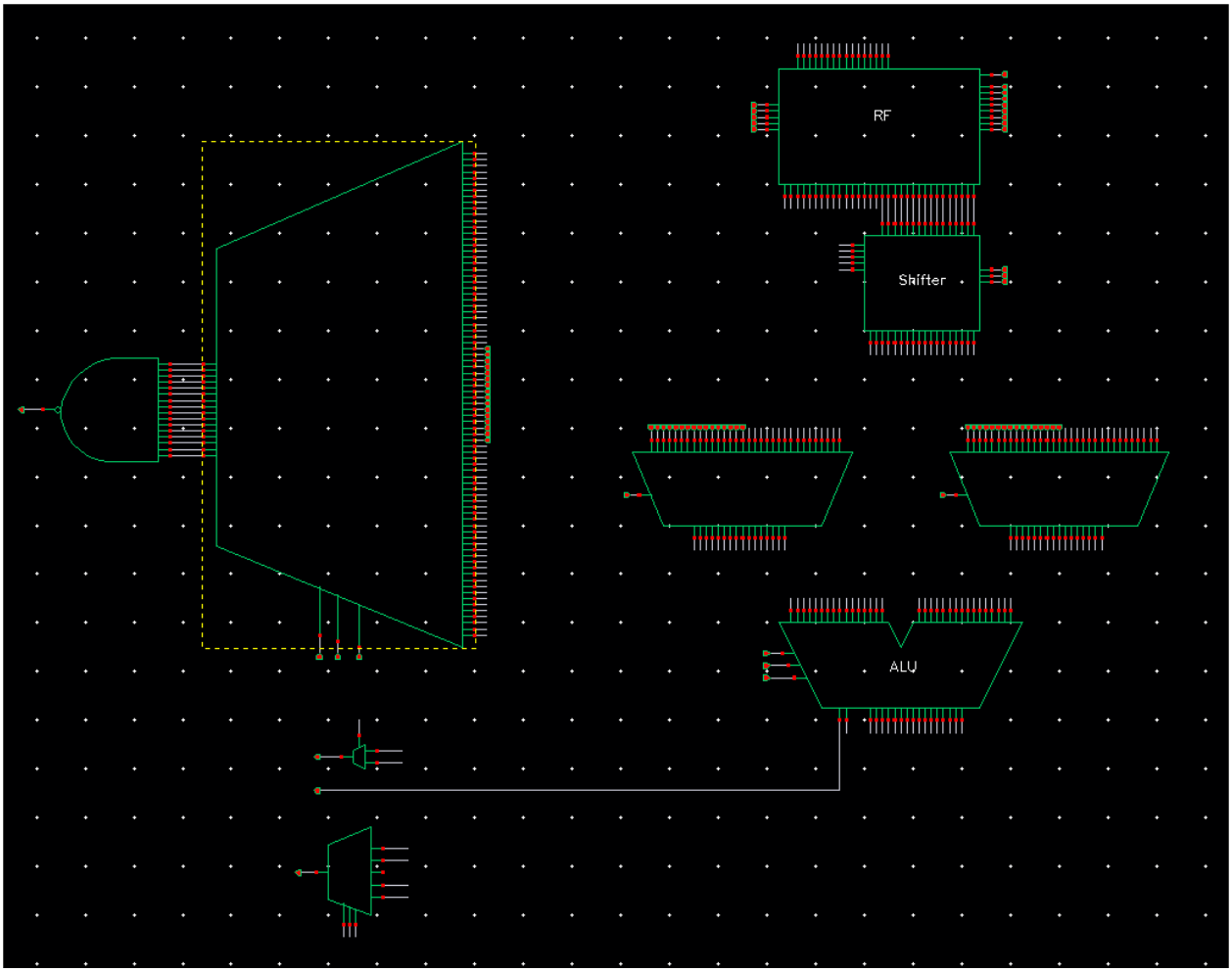

Figure 3.3 Schematic Design of the Data Path

4. Layout

Figure 4.1 shows the layout design of the data path which also passed DRC and LVS. Figure 4.2 and Figure 4.3 shows the DRC and LVS report of our post-layout.

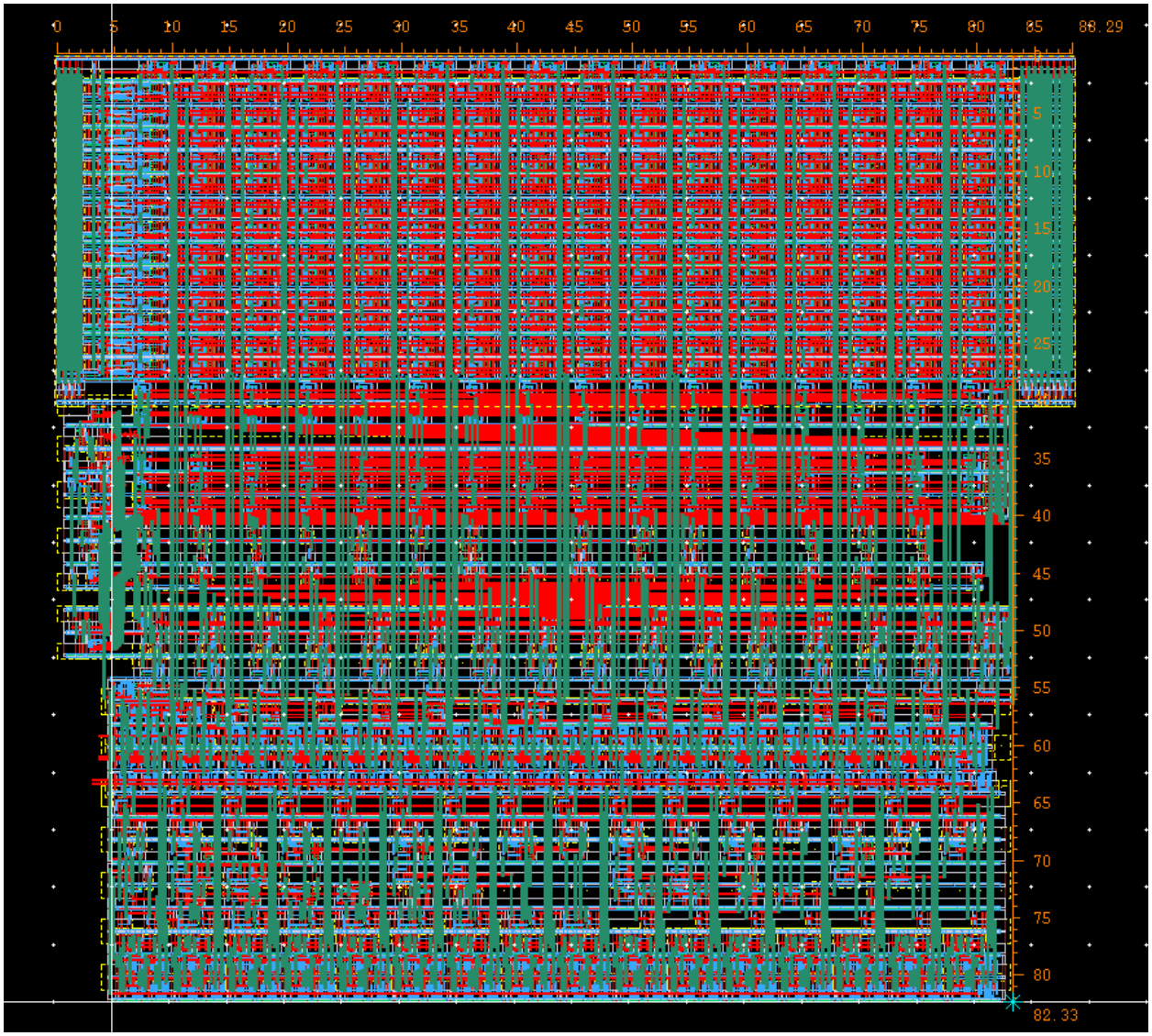

Figure 4.1 Post- layout Design of the Data-path

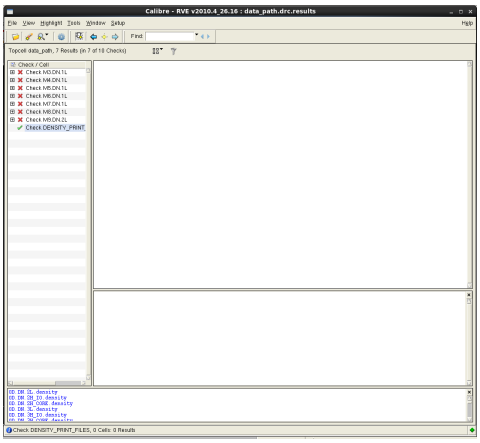

Figure 4.2 DRC Report

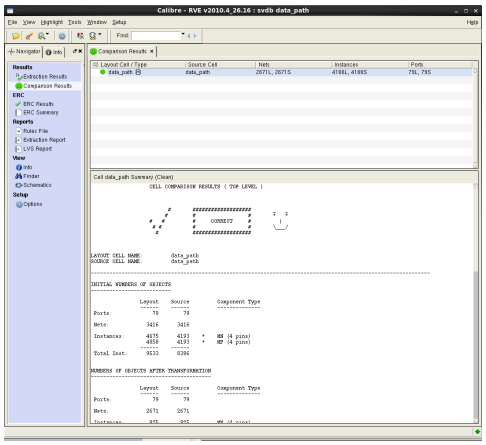

Figure 4.3 LVS Report

5. Verification

In order to verify that our data path is functionally correct. We test different cases of operations.

1: Each cycle, take in input from imm0 and store them in the address 1 and address 2 in the register file. Then use these use these two data to perform the addition in the ALU. And finally, select this output to the result. And in this operation, the shifter output is also correct. Figure 5.1 shows the complete operation waveform.

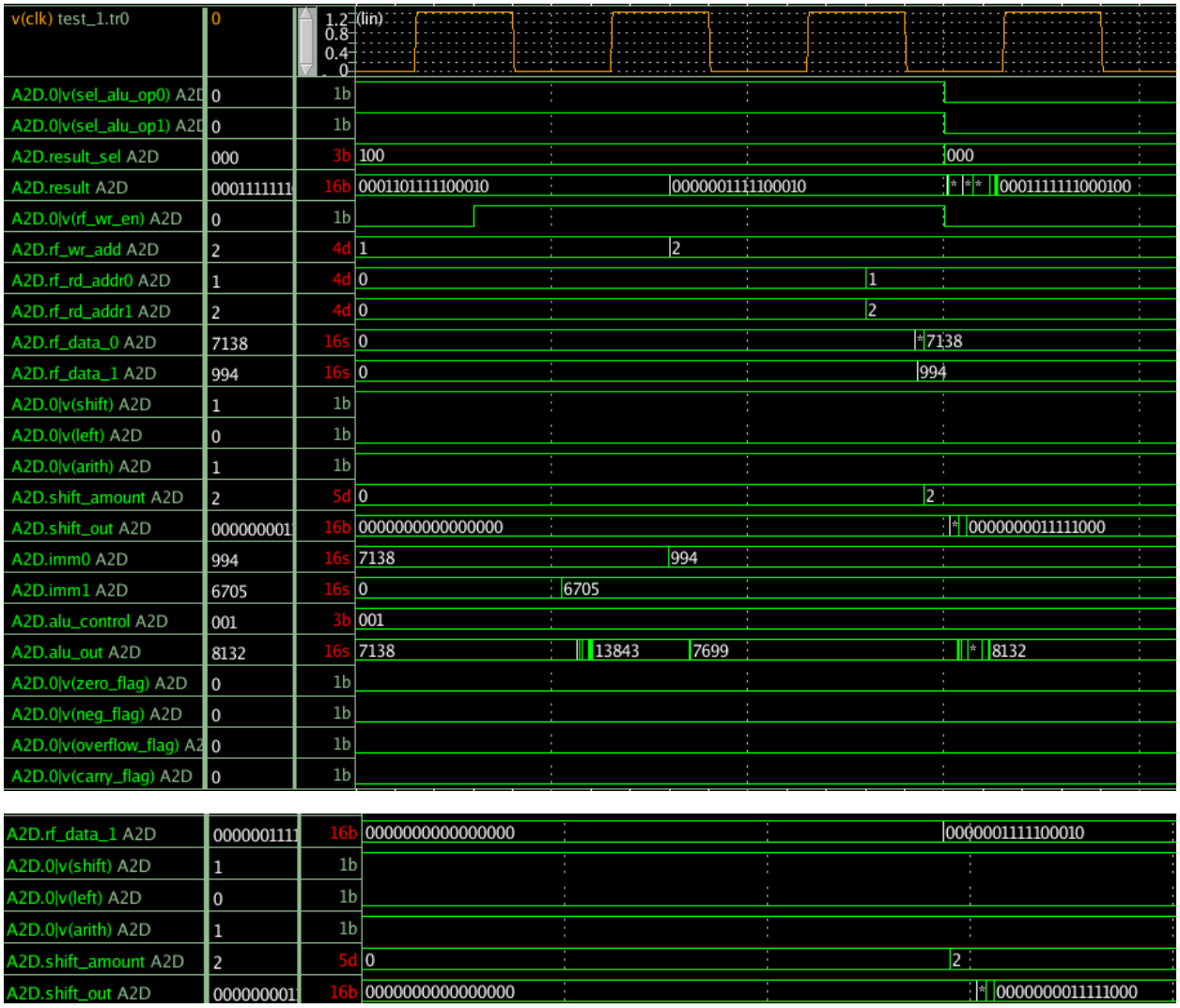

Figure 5.1 - test-1 complete operation waveform

6. Measurements and Analysis

Critical Path

The critical path of the schematic design starts from the read_address input of register file, goes to operand selection for ALU, after addition or subtraction operations, it goes to result selection mux, then end in zero-detector. The post-layout has the same critical path as the schematic design.

	Schematic Design:	Post Layout
Critical Delay	915 ps	1.63 ns

Layout Size:

Width: 88.29,

Height: 82.33,

Area: 7268.9

Aspect Ratio: 1.07

7. Directory

"/home/projects/ee477/yuxiangc/cad5/results"

Schematic:

- Control file: data_path_schematic.ctl
- Netlist file: data_path_schematic.ckt
- Waveform: data_path_schematic.tr0

Layout:

- Control file: data_path_layout.ctl
- Netlist file: data_path_layout.ckt
- Simulation: data_path_layout.tr0
- Pex: data_path.pex.netlist / data_path.pex.netlist.DATA_PATH.pxi
- drc: /drc
- lvs: /lvs