High-speed low-power 2D DCT Accelerator

EECS 6321
Yuxiang Chen, Xinyi Chang, Song Wang
Electrical Engineering, Columbia University
Prof. Mingoo Seok

Project Goal

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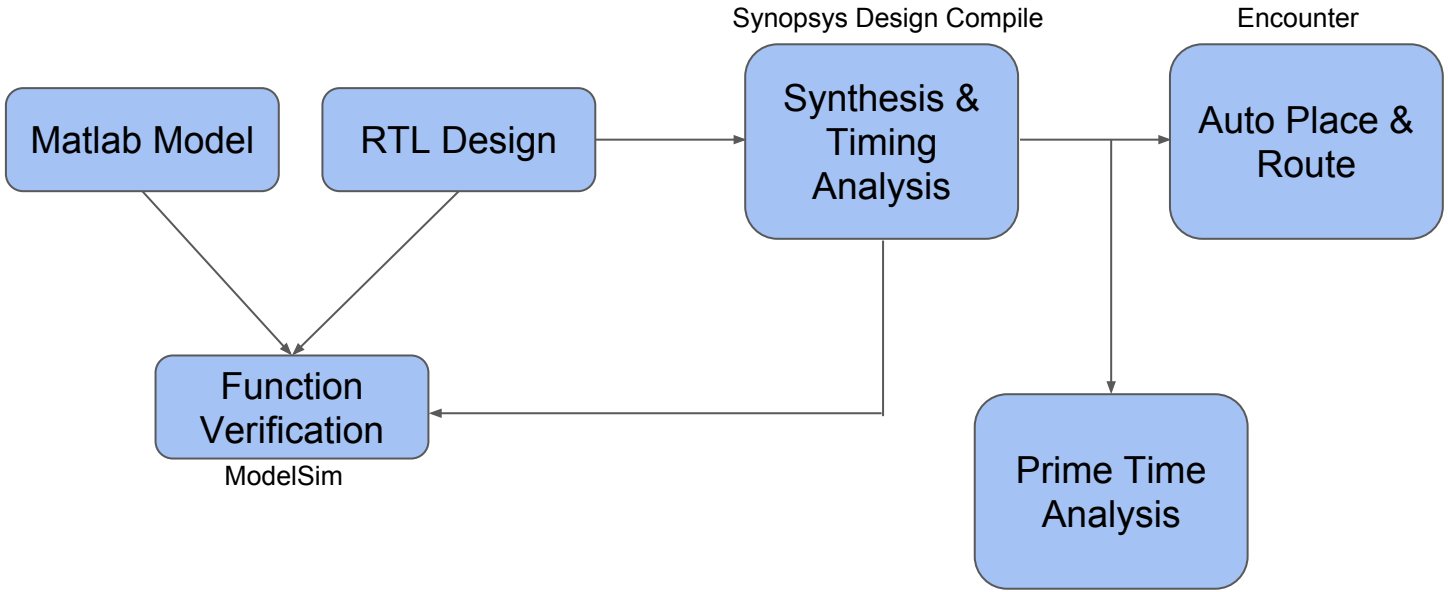
- Execute a full VLSI design flow from RTL design to place and route with custom standard cell.
- Demonstrate a low power design methodology using standard tool flows

Steps

- Matlab implementation of DCT algorithm utilizing
- RTL Implementation of DCT and Approximate Adder, tested using matlab generated random inputs.
- Approximate Adder Physical Layout with standard cell dimensions
- Synthesize/post-synthesize RTL to gate level netlist. Measured delay and power
- APR with IBM 130nm standard cell and APPROX_ADDER cell.
- Fixed DRC errors. LVS Free.

Methodology Overview



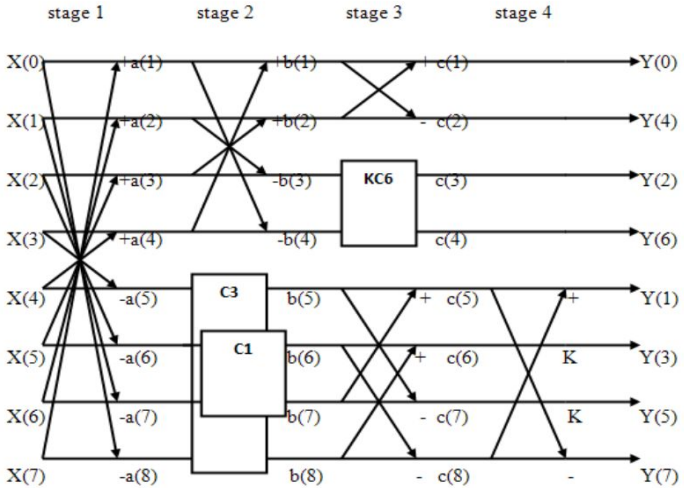
DCT with Loeffler Algorithm

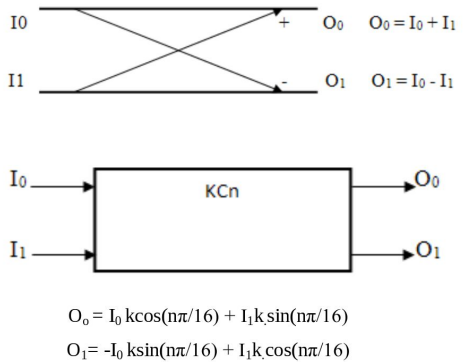
$$y(k) = w(k)\sum_{n=1}^{N} x(n)\cos\left(\frac{\pi}{2N}(2n-1)(k-1)\right), \quad k = 1, 2, \ldots, N,$$

$$w(k) = \begin{cases} \frac{1}{\sqrt{N}}, & k = 1, \\ \sqrt{\frac{2}{N}}, & 2 \le k \le N, \end{cases}$$

Loeffler Algorithm

- Number of multiplications reach the theoretical low limit.
- 4 Stages
- MultAddSub Blocks





$$O_o = I_0\, k\cos(n\pi/16) + I_1 k \sin(n\pi/16)$$

$$O_1 = -I_0\, k\sin(n\pi/16) + I_1 k \cos(n\pi/16)$$

[1]M. Jridi and A. Alfalou,

Canonical signed digit (CSD) representation

$$y(k) = w(k)\sum_{n=1}^{N} x(n)\cos\left(\frac{\pi}{2N}(2n-1)(k-1)\right), \quad k = 1, 2, \ldots, N, \qquad w(k) = \begin{cases} \frac{1}{\sqrt{N}}, & k = 1, \\ \sqrt{\frac{2}{N}}, & 2 \le k \le N, \end{cases}$$

CSD

- Signed representation containing the fewest number of nonzero bits
- Effective way to carry out constant multiplier for DCT.
- Number of additions and subtractions will be minimized.
- Identified common elements in CSD constant coefficients and shared required resource

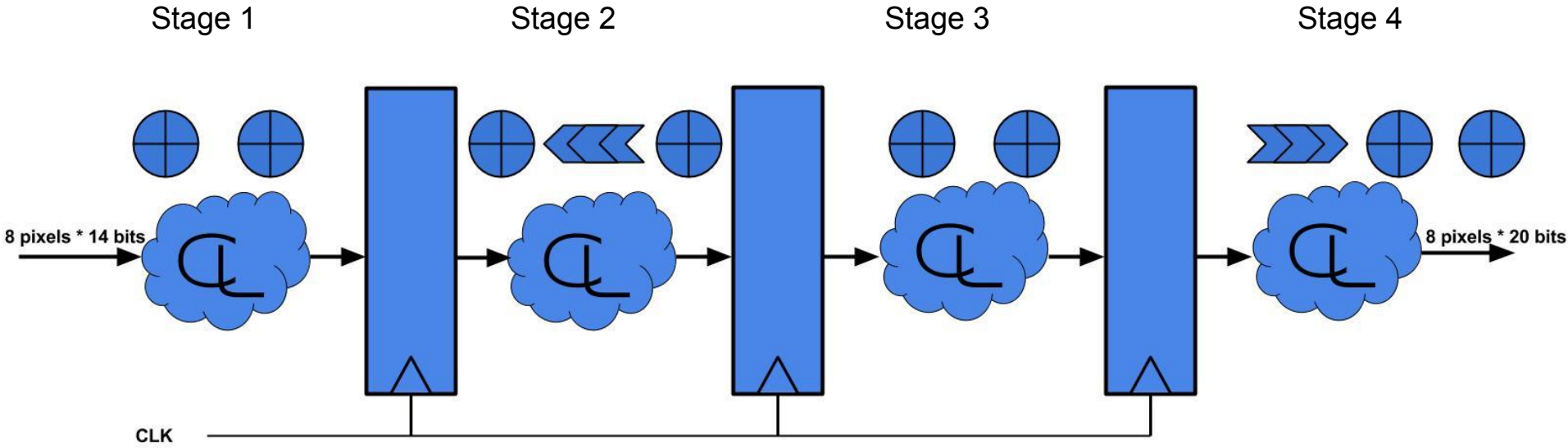
X = 2^a ± 2^b ± 2^c ±…..

TABLE I
8-POINT DCT FIXED COEFFICIENT REPRESENTATION

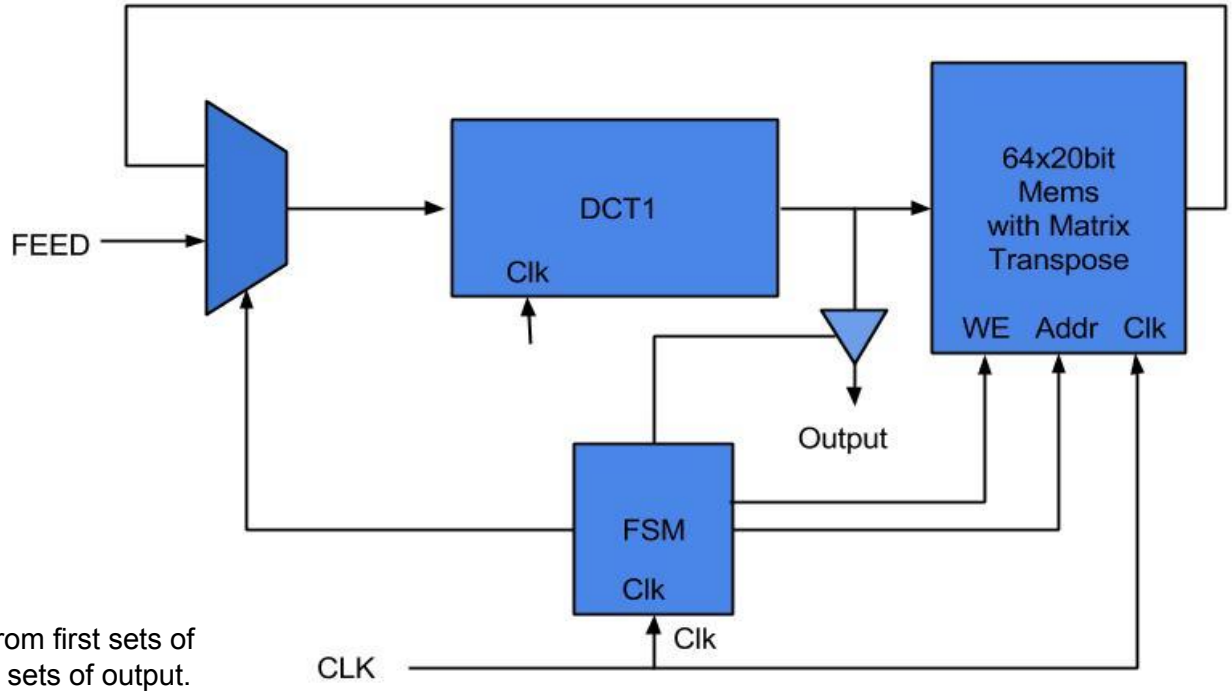
Real value	Decimal	Natural binary	Partial products	CSD	Partial products
$cos\frac{3\pi}{16}$	106	01101010	4	+0-0+0+0	4
$sin\frac{3\pi}{16}$	71	01000111	4	0+00+00-	3
$cos\frac{\pi}{16}$	126	01111110	6	+00000-0	2
$sin\frac{\pi}{16}$	25	00011001	3	00+0-00+	3
$cos\frac{6\pi}{16}$	49	00110001	3	0+0-000+	3
$sin\frac{6\pi}{16}$	118	01110110	5	+000-0-0	3
$\sqrt{(2)}$	181	10110101	5	+0-0-0+0+	5
Total Partial products		30		23	

[1]M. Jridi and A. Alfalou,

RTL Block Diagram for DCT-1

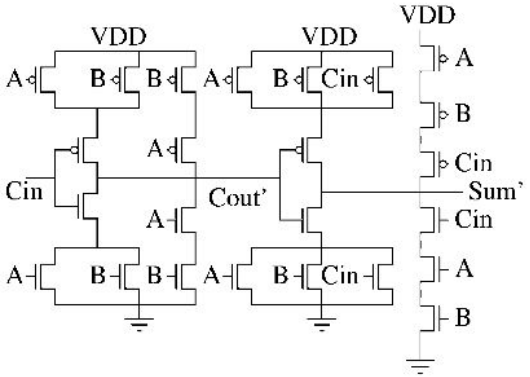


RTL Block Diagram for DCT-2

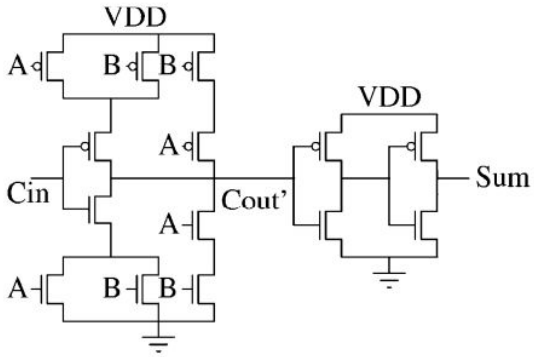


- 21 Cycles from first sets of input to last sets of output.
- Data feeds every 19 cycles

Semi-custom Approximate Adder



conventional MA



approximate adder

- Removal of some series connected transistors will facilitate faster charging/discharging of node capacitances.
- Complexity reduction by removal of transistors also aids in reducing dynamic power .
- Use approximate FA cells only in LSBs , thus ensuring that the final output quality does not degrade too much
- Measure the output quality using MSE (mean square error)

[3] V. Gupta, D. Mohapatra, A. Raghunathan and K. Roy

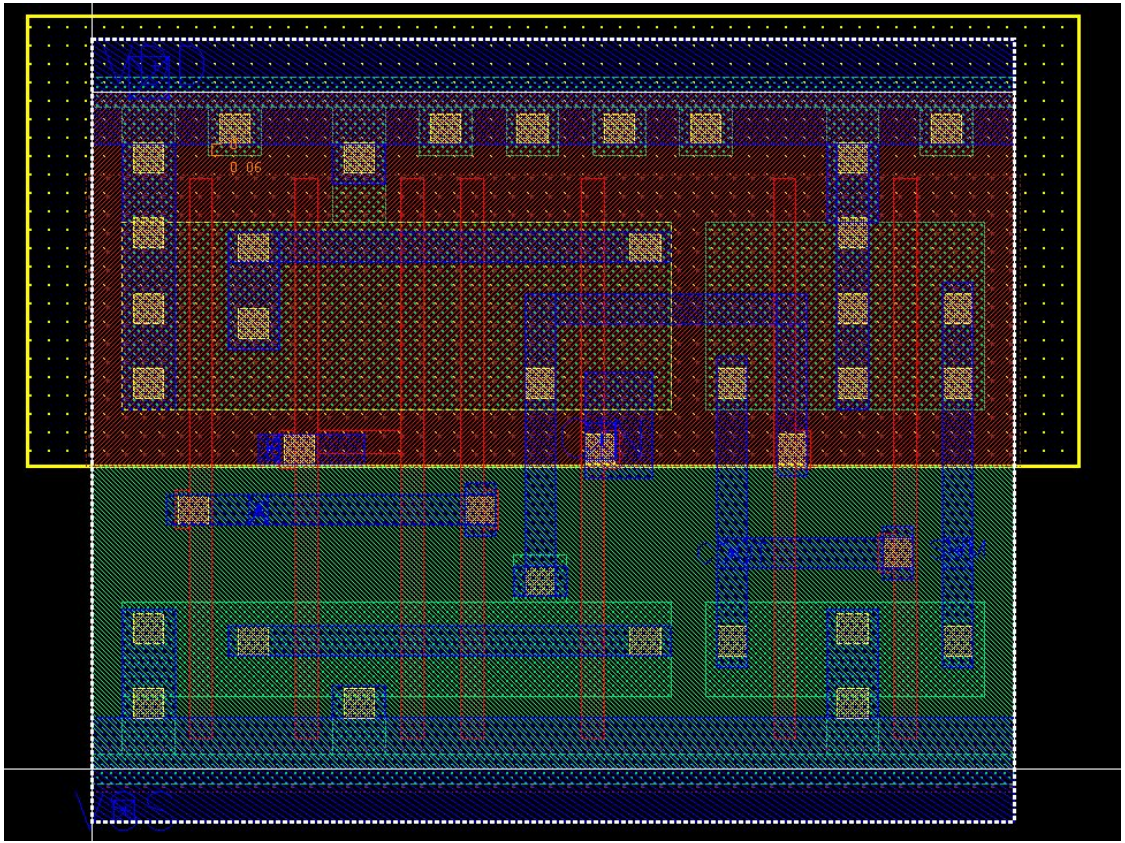
Design Compiler

- Combine scx3_cmos8rf_lpvt_tt_1p2v_25c.db and cmrf8sf_custom.db to synthesize the whole design
- Set_don’t_touch our customized cell approximate adder
- Use the smallest driven cell INVXLTS for all the inputs to get the maximum optimization

Netlist Simulation

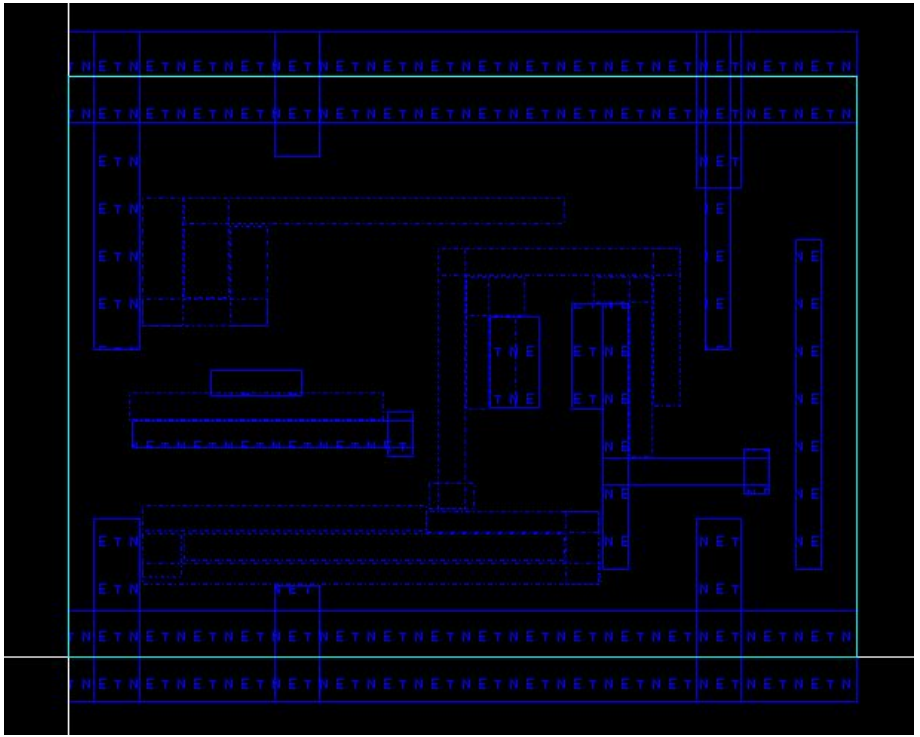
- Simulate the function and timing in modelsim

Semi-custom Approximate Adder

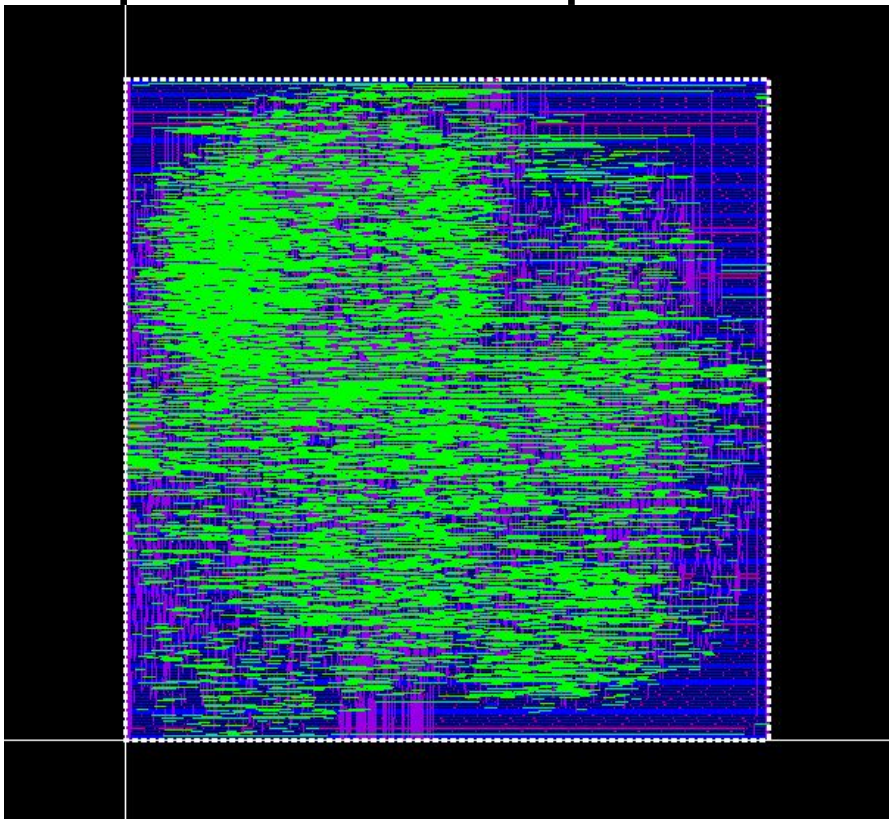


Abstract View

- Detailed Blockage abstract
- Draw blockage manually to mitigate defects of APR tool



Floorplan - final Implementation



Size: 710.2 (W) x 730.2 (H)

Challenges:

- Match custom cell boundary to power grid.
- Antenna Issue.
- APR routing challenge.

Approximate Adder Accuracy Comparison

Number of Approximate Adder	MSE	PSNR
1	3.53	42.68 dB
2	13.46	36.87 dB
3	41.95	31.94 dB

Result

With Adder	A	B	C
Total Power (mW)	70.753	66.254	63.899
Area (um^2)	191558.88	182021.76	174057.11
Frequency (ns)	225.7	225.7	225.7

State of the Art	Power (mW)	Area (mm^2)
DCT Core	29.92	0.569

Adder A: RCA with full adders.
Adder B: RCA with LSB 3 bits synthesized approximate adder.
Adder C: RCA with LSB 3 bits customized approximate adder.

Reference

[1] M. Jridi, A. Alfalou, "A low-power, high-speed DCT architecture for image compression: Principle and implementation," 18th IEEE/IFIP VLSI System on Chip Conference (VLSI-SoC), 2010, pp. 304-309.

[2] Y. H. Chen , T. Y. Chang and C. Y. Li , "Highthroughput DA-based DCT with high accuracy error-compensated adder tree" , IEEE Trans. VeryLarge Scale Integr. (VLSI) Syst. , vol. 19 , no. 4 , pp.709 -714 , 2011

[3] V. Gupta, D. Mohapatra, A. Raghunathan and K. Roy , "Low-power digital signal processing using approximate adders" , IEEE Trans. Comput.-Aided Design Integr. Circuits Syst. , vol. 32 , no. 1 , pp.124 -137 , 2013

[4] P. Kulkarni, P. Gupta, and M. D. Ercegovac, “Trading accuracy for power in a multiplier architecture,” J. Low Power Electron., vol. 7, no. 4, pp.490–501, 2011.

[5] Y. V. Ivanov and C. J. Bleakley, “Real-time h.264 video encoding in software with fast mode decision and dynamic complexity control,” ACM Trans. Multimedia Comput. Commun. Applicat., vol. 6, pp. 5:1–5:21, Feb. 2010.