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Phase noise analysis in CMOS differential Armstrong oscillator topology

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SUMMARY

This paper reports a phase noise analysis in a differential Armstrong oscillator circuit topology in CMOS technology. The analytical expressions of phase noise due to flicker and thermal noise sources are derived and validated by the results obtained through SpectreRF simulations for oscillation frequencies of 1, 10, and 100 GHz. The analysis captures well the phase noise of the oscillator topology and shows the impact of flicker noise contribution as the major effect leading to phase noise degradation in nano-scale CMOS LC oscillators. Copyright © 2016 John Wiley & Sons, Ltd.

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KEY WORDS: Armstrong oscillator topology; CMOS integrated circuits; microwave and millimeter waves; phase noise circuit analysis; transformer

1. INTRODUCTION

The phase noise performance of the local oscillator is one of the most critical bottlenecks in modern radio transceivers. Despite significant advances in recent years, achieving low-phase noise is still a significant challenge [1–5].

Numerical methods for predicting accurately phase noise are not always available. However, even when such methods exist, in design environments such as Cadence, they may not provide the necessary insights to the designer. Thereby, relatively simple and intuitive analytical expressions are desirable in order to provide a first-order yet accurate prediction of phase noise in oscillator circuit topologies [6, 7].

In this regard, a linear time-variant model based on the impulse sensitivity function (ISF) was introduced in [8], which describes the phase sensitivity to noise perturbations. The ISF approach was found very helpful for getting critical insights about oscillator phase noise and was used widespread over the past years. As examples, in [9], it was adopted to derive phase noise expressions for differential Colpitts and common-source cross-coupled oscillators. Its application on the tuned-input-tuned-output and injection-locked oscillators was presented in [10] and [11], respectively.

Another approach for deriving accurate expressions of the phase noise is based on phasor analysis. In particular, expressions for the noise of the output spectrum of common-source single and double cross-coupled oscillator circuit topologies were derived in [12, 13].

As examples, analytical derivations of phase noise in multiphase and quadrature voltage controlled oscillators have been reported in [14, 15]; phase noise analyses in ring oscillators

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have been addressed in [16–19]; moreover, phase noise in relaxation oscillators has been studied in [18, 20, 21].

In our previous studies [22–24], the differential Armstrong oscillator circuit topology was compared in terms of phase noise performance with common-source cross-coupled, Colpitts, and Hartley differential circuit topologies at operating frequencies in the range from 1 to 100 GHz. The differential Armstrong topology proposed therein exploits integrated transformers [25–27] in order to implement magnetic coupling between the gate and drain terminals of the transistor pair in the oscillator. Under the adopted design conditions, common to all topologies, the Armstrong topology showed a good potential for superior phase noise performance in the oscillation frequency range from 1 to 20 GHz. Moreover, in this oscillation frequency range, the $1/f^3$ phase noise corner for the differential Armstrong topology was reported to be smaller with respect to the other examined topologies. This means that this oscillator topology shows a high potential for applications with more stringent phase noise requirements in low-frequency offsets, thanks to its reduced up-conversion of low-frequency noise.

As a consequence to our previous studies, an in-depth investigation of phase noise is in order, because it may allow us to obtain useful insights and drive through accurate and optimized circuit design. Thereby, from a designer perspective, such an analysis could be very helpful in focusing the design efforts toward specific directions.

To date, to the best of our knowledge, an in-depth study of phase noise in Armstrong oscillator circuit topology, either differential or not, through analytical investigations of phase noise has not been addressed yet in the literature.

In this paper, we address a complete analytical study of phase noise in the differential Armstrong topology shown in Figure 1, with the objective of providing a closed-form symbolic expression for the phase noise by using the ISF. In detail, in this paper, we report a theoretical analysis of the phase noise exhibited by the differential Armstrong oscillator topology shown in Figure 1, in both the $1/f^3$ and $1/f^2$ regions. The analytical expressions derived by our theoretical study are then validated through the comparison with the results of the circuit simulations carried out within the Cadence design environment, which takes into account the full models of the transistors of a process design kit commercially available, including all their parasitic components. In compliance with the expectations from the theoretical study, in our analyses, we will exclude the effects of the layout interconnections; moreover, it is worth considering that the additional parasitic components introduced by the layout could lead to an unwanted increase of complexity and cumbersome expressions, which could mask the topological properties that we would like bringing to the light in our study. Capacitors will be considered as ideal components, whereas a typical quality factor (Q) of 10 is considered for all the spiral inductors. The assumptions made previously are reasonable in a first-order approximation and in line with the common practice adopted by other theoretical

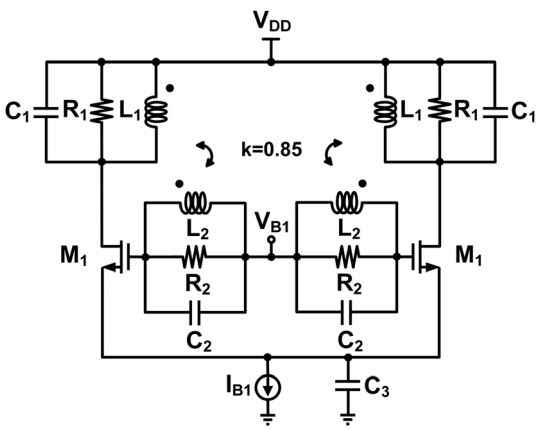

Figure 1. Schematic of the differential Armstrong oscillator circuit topology. V_{B1} and I_{B1} are direct current bias voltage and current sources, respectively.

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studies reported in the literature. From the comparison with the simulation results, we will see that the results of our study are characterized by a good accuracy.

The paper is organized as follows. Section 2 reports the analysis of phase noise for the differential Armstrong topology of Figure 1. In Section 3, the theoretical results are validated by the results obtained from SpectreRF simulations for the oscillation frequencies of 1, 10, and 100 GHz. Finally, conclusions are drawn in Section 4.

2. PHASE NOISE ANALYSIS

Figure 1 shows the differential Armstrong oscillator circuit topology designed in 28 nm bulk CMOS technology with 1 V supply voltage. In order to make the results directly comparable with those of our previous works, the oscillator circuit design has been carried out with the same transistor size, power, and current consumptions, inductance of the tanks, and their quality factors, as in [22–24]. In particular, the width of transistor pair M_1 is 15 μm. The direct current (dc) bias voltage and current sources V_{B1} and I_{B1}, respectively, in Figure 1 are chosen such that the total power consumption is 6.3 mW for all oscillation frequencies. In addition, a coupling factor k of 0.85 is assumed for the transformers. In order to exclude noise from the bias circuitry being converted to phase noise, V_{B1} and I_{B1} are chosen to be ideal and noiseless. This will allow a direct verification of the theoretical analysis carried out in Section 2 with the SpectreRF simulation results reported in Section 3.

In our study, we aim at extending the analysis to the $1/f^3$ phase noise region, not addressed yet in the literature, because such an analysis would be essential in order to achieve a good phase noise prediction in oscillator topologies designed in deep submicron (nano-scale) technologies. Indeed, flicker noise in the output spectrum of an integrated CMOS oscillator is particularly important because the $1/f^3$ phase noise region usually extends beyond 1 MHz offset from the oscillation frequency, as a consequence of nano-scale devices featuring 1/f corner frequencies of several tens or hundreds of megahertz.

In order to have expressions in a more manageable form, in an analogy with [10], it is convenient to change the ground reference as shown in Figure 2. By using the describing function approach [28], we achieve the single-ended large-signal equivalent circuit shown in Figure 3.

I_1 is the amplitude of the fundamental harmonic of the drain current of M_1. Denoting the drain and gate resonator impedances as Z_D and Z_G, respectively, n is defined as the ratio $Z_G/(Z_D+Z_G)$. C_{GD} is the large-signal capacitance between gate and drain of M_1, which can be either a parasitic component or external to the transistor itself. C_{1eq} represents the parallel combination of C_1 with

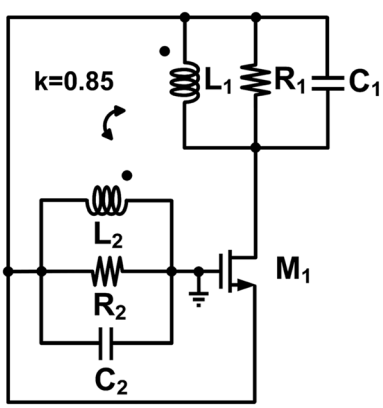

Figure 2. Single-ended large-signal equivalent circuit of the differential Armstrong oscillator circuit topology of Figure 1, with changed ground reference.

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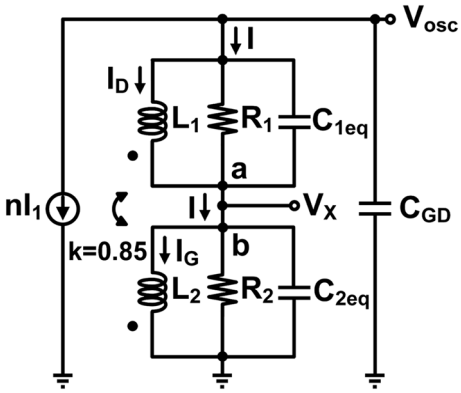

Figure 3. Single-ended large-signal equivalent circuit of the differential Armstrong oscillator circuit topology of Figure 1, based on the describing-function approach.

the large signal drain-to-bulk capacitance C_{DB} of M_1, whereas C_{2eq} is the parallel combination of C_2 with the large-signal gate-to-source capacitance C_{GS} of M_1.

Defining M as $k\sqrt{L_1 L_2}$ and Z_1, Z_2 as the impedances given by the parallel combination of R_1, C_{1eq} and R_2, C_{2eq}, respectively

$$Z_1 = \frac{R_1}{1 + sR_1 C_{1eq}} \tag{1}$$

$$Z_2 = \frac{R_2}{1 + sR_2 C_{2eq}} \tag{2}$$

we can write

$$V_{osc} - V_X = L_1 s I_D + I_G M s \tag{3}$$

$$V_X = L_2 s I_G + I_D M s \tag{4}$$

From Kirchhoff current law (KCL) at the output node

$$I = -nI_1 - V_{osc} s C_{GD} \tag{5}$$

Moreover, from KCL at nodes a and b, respectively

$$I_D = I - \frac{V_{osc} - V_X}{Z_1} \tag{6}$$

$$I_G = I - \frac{V_X}{Z_2} \tag{7}$$

Then we use (5) into (6) and (7) in order to write I_D and I_G as function of V_{osc} and V_X, respectively, as follows:

$$I_D = -nI_1 - V_{osc} s C_{GD} - \frac{V_{osc} - V_X}{Z_1} \tag{8}$$

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$$I_G = -nI - V_{osc} s C_{GD} - \frac{V_X}{Z_2} \tag{9}$$

Using (8) and (9) into (3) and (4), we can express V_{osc} and V_X as a function of circuit components with known values. Afterwards, expressing Z_D and Z_G as $(V_{osc} - V_X)/I$ and V_X/I, respectively, and then summing, we yield

$$Z_D + Z_G = \frac{\left(L_1 L_2 - M^2\right)(Z_1 + Z_2)s^2 + Z_1 Z_2 (L_1 + L_2 + 2M)s}{(L_1 L_2 - M_2)s^2 + (L_1 Z_2 + L_2 Z_1)s + Z_1 Z_2} \tag{10}$$

$Z_D + Z_G$ can be interpreted as a parallel RLC resonator made of an inductance $L_T = L_1 + L_2 + 2M$, a resistance $R_T = R_1 + R_2$, and a capacitance $C_p = C_{GD} + C_{1eq} C_{2eq}/(C_{1eq} + C_{2eq})$ [10].

We now define $\Gamma_{eff,rms}$ and $\Gamma_{eff,dc}$ as the root mean square (rms) and dc values of the effective ISF for the noise current of M_1 [8, 9]. Using $\Gamma^2_{eff,rms}$ in (21) and $\Gamma^2_{eff,dc}$ in (23) from [8], as corrected in [29], and equating we find

$$\Gamma^2_{eff,dc} = \frac{\omega_{1/f^3}}{\omega_{1/f}} \Gamma^2_{eff,rms} \tag{11}$$

where ω_{1/f^3} is the frequency where the sideband power due to thermal noise is equal to the sideband power due to flicker noise, and $\omega_{1/f}$ is the corner frequency of the flicker noise generated by M_1. From [9], $\Gamma^2_{eff,rms}$ is given by

$$\Gamma^2_{eff,rms} = \frac{(1-n)^2}{N^2} \frac{I_1}{2\left(\mu_n C_{ox} \frac{W}{L}\right) V_1^2} \tag{12}$$

where C_{ox} is the gate oxide capacitance per unit area approximately equal to 0.026 F/m^2, W and L are the width and length of M_1, respectively, and V_1 is the amplitude of the fundamental harmonic of the source voltage of M_1.

The phase noise due to flicker noise from M_1 can be written as

$$\mathcal{L}(\Delta\omega)\Big|_{flicker} = N \frac{1}{2 q_{max}^2 \Delta\omega^2} \Gamma^2_{eff,dc} \frac{\overline{i_n^2}}{\Delta f} \frac{1}{(\cos\phi - \cos\Phi)^2} \tag{13}$$

where $N = 2$ for the differential Armstrong, q_{max} is the maximum charge displacement across the tank capacitance equal to $V_{tank} \times C_p$, V_{tank} being the amplitude of the fundamental harmonic of the tank voltage. $\Delta\omega$ is the angular frequency offset from the oscillation frequency, and Φ is half the conduction angle defined by

$$\Phi = \cos^{-1}\left(\frac{V_{GS} - V_T}{V_1}\right) \tag{14}$$

where ϕ is equal to ω_0t, V_{GS} is the dc gate-to-source voltage of M_1, and V_T is the threshold voltage of M_1. Also, $\overline{i_n^2}/\Delta f$ is the power spectral density of the flicker noise current of M_1 reported in [30, 31]

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{K g_{m1}^2}{C_{ox} W L} \frac{1}{f} \tag{15}$$

where K is a process-dependent constant approximately equal to 10^{-23} V^{2}F, f is the frequency, and g_{m1} is the small-signal transconductance of M_1 given by

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$$g_{m1} = \left(\mu_n C_{ox} \frac{W}{L}\right) V_1 (\cos\phi - \cos\Phi) \tag{16}$$

where μ_n is the electron mobility approximately equal to $0.06\,\mathrm{m}^2/(V \times s)$.

Moreover, from [28], we can write

$$V_1 = I_1 \frac{R_T n}{n^2 G_{m1} R_T + 1} \tag{17}$$

$$V_{tank} = \frac{V_1}{n} \tag{18}$$

where G_{m1} is the large-signal transconductance of M_1 equal to I_1/V_1.

Also, from [9], g_{m1} is proportional to G_{m1}

$$G_{m1} = \frac{2}{15\pi}\Phi^5 \left(1 - \frac{11}{42}\Phi^2\right) \frac{1}{(\cos\Phi - \cos\phi)} g_{m1} \tag{19}$$

The phase noise given by (13) can now be rewritten as

$$\mathcal{L}(\Delta\omega)\Big|_{flicker} = \frac{\pi(1-n)^2 K \mu_n}{2N} \frac{\omega_{1/f^3}}{\omega_{1/f}} \frac{1}{\Delta\omega^3} \frac{n^2 G_{m1} R_T + 1}{V_{tank} R_T C_p^2 L^2} \tag{20}$$

It is worth noting that, as it could be expected intuitively, a higher V_{tank} will result in lower flicker noise from M_1 being up-converted into phase noise. Moreover, (19) and (20) suggest that the larger the excess gain $g_{m1}R_T$, the more pronounced is the flicker noise up-conversion. This can be attributed to the increase of the harmonic distortion of the output voltage, because of noise current tones modulating the amplitude of the voltage harmonics. In turn, this effect causes changes in the oscillation frequency, thereby producing phase noise as explained in [32].

Phase noise due to thermal noise can be expressed as [9, 10]

$$\mathcal{L}(\Delta\omega)\Big|_{thermal} = \frac{K_B T \left(1 + \gamma \frac{1-n}{n}\right)}{V_{tank}^2 C_p^2 \Delta\omega^2 R_T} \tag{21}$$

where K_B is the Boltzmann constant, T is the absolute temperature, and γ is the excess noise coefficient.

The overall phase noise is given by

$$\mathcal{L}(\Delta\omega)\Big|_{total} = 10\log_{10}\left[\mathcal{L}(\Delta\omega)\Big|_{flicker} + \mathcal{L}(\Delta\omega)\Big|_{thermal}\right] \tag{22}$$

In the next section, the phase noise predicted by (20–22) will be compared with the results from circuit simulations carried out within the Cadence design environment.

3. NUMERICAL EVALUATIONS AND CIRCUIT SIMULATIONS

For simplicity, we assume that the drain and gate resonators are identical, neglecting the possible slight difference in parasitic capacitance in the resonators. This means that n is a real number and equal to 0.5. As in [22–24], L_1 and L_2 are chosen equal to 5 nH, 500 pH, and 50 pH for the oscillation frequencies of 1, 10, and 100 GHz, respectively.

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Assuming that the losses due to the parasitic resistance of the inductors L_1 and L_2 dominate the losses in the drain and gate resonators, the parasitic resistors R_1 and R_2 are equal to $QL_1\omega$ and $QL_2\omega$, respectively. Q is equal to 10, and ω is the angular frequency of operation. C_1 and C_2 are equal to 2.5 pF, 231 fF, and 8 fF for the operating frequencies of 1, 10, and 100 GHz, respectively. C_3 is equal to 1 μF, in order to exhibit small impedance toward ground at the frequency of oscillation.

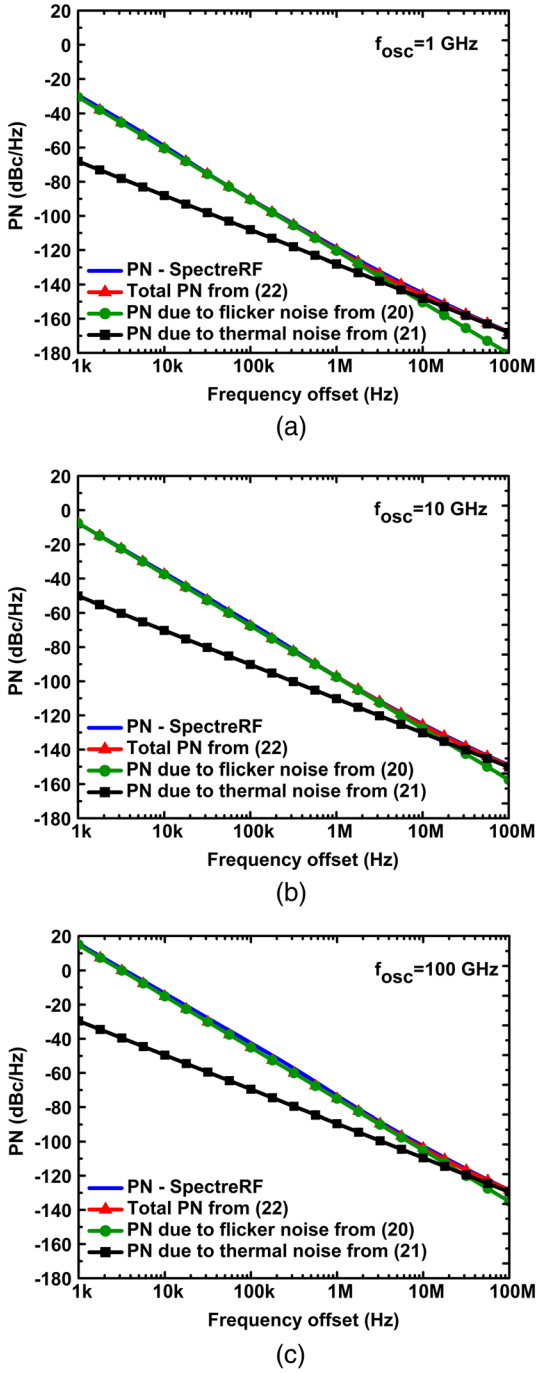

Figure 4. Phase noise (PN) versus frequency offset obtained from direct plots through PSS and Pnoise SpectreRF simulations, as well as from the theoretical expressions of (20–22) for an oscillation frequency of: (a) 1 GHz; (b) 10 GHz; and (c) 100 GHz.

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Figure 4 shows the phase noise obtained by direct plots from periodic steady state (PSS) and periodic noise circuit simulations in SpectreRF, for oscillation frequencies of 1, 10, and 100 GHz. Phase noise is reported over a wide frequency offset from the carrier frequency, in order to include the regions in which the noise at the output spectrum is dominated by either flicker or thermal noise.

Figure 4 reports also the numerical evaluations of the theoretical expressions of phase noise due to flicker and thermal noise from (20) and (21), respectively, as well as the total phase noise from (22). Note that the theoretical phase noise predicted by (20–22) matches well with the results obtained by means of SpectreRF simulations. Even for the oscillation frequency of 100 GHz, where the worst match is observed, the theoretical phase noise predicted by (22) is within 3 dB difference from the simulation results.

In all cases considered here, the $1/f^3$ frequency corner is beyond 1 MHz frequency offset. In particular, it is at the frequency offset of 5.8, 18, and 28 MHz from the oscillation frequencies of 1, 10, and 100 GHz, respectively. These last results confirm the rising role of flicker noise in oscillators designed in a nano-scale CMOS technology, as already shown in [22–24]. This means that the devices with the largest contribution to the flicker noise component of phase noise will also dominate phase noise.

4. CONCLUSIONS

This paper reports, for the first time, a theoretical analysis of the phase noise in a differential Armstrong oscillator circuit topology, both in the $1/f^3$ and $1/f^2$ regions, in order to allow accurate predictions.

Flicker noise up-conversion has resulted explicitly linked to the excess gain of the oscillator circuit topology. Specifically, because of the non-linear nature of the topology, larger excess gain causes more flicker noise from the active devices in the circuit being up-converted near the oscillation frequency.

The derived analytical expressions of the phase noise have been validated through a direct comparison with the results obtained by SpectreRF simulations for a discrete set of oscillation frequencies spanning over two decades from 1 to 100 GHz. Under the adopted design conditions, the theoretical and simulation results are in a good agreement, with a maximum deviation of about 3 dB at 100 GHz.

Finally, the analysis of the results obtained by the theoretical derivations allowed us to identify the dominant noise contributions. It can be observed that in all cases, the flicker noise from the active devices is the component with the most significant effect in terms of phase noise on the oscillator output spectrum at 1 MHz offset from the carrier frequency.

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