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Analyses and techniques for phase noise reduction in CMOS Colpitts oscillator topology

Ilias Chlis[1,2], Domenico Pepe[1] and Domenico Zito[1,2,*†]

[1]*Marconi Lab, Tyndall National Institute, Lee Maltings, Dyke Parade, Cork, Ireland*
[2]*Department of Electrical and Electronic Engineering, University College Cork, College Road, Cork, Ireland*

SUMMARY

This paper reports the analyses of three techniques for phase noise reduction in the complementary metal-oxide semiconductor (CMOS) Colpitts oscillator circuit topology. Namely, the three techniques are inductive degeneration, noise filter, and optimum current density. The design of the circuit topology is carried out in 28-nm bulk CMOS technology. The analytical expression of the oscillation frequency is derived and validated through circuit simulations. Moreover, the theoretical analyses of the three techniques are carried out and verified by means of circuit simulations within a commercial design environment. The results obtained for the inductive degeneration and noise filter show the existence of an optimum inductance for minimum phase noise. The results obtained for the optimum bias current density technique applied to a Colpitts oscillator circuit topology incorporating either inductive degeneration or noise filter show the existence of an optimum bias current density for minimum phase noise. Overall, the analyses show that the adoption of these techniques may lead to a potential phase noise reduction up to 19 dB at a 1-MHz frequency offset for an oscillation frequency of 10 GHz. © 2015 The Authors International Journal of Circuit Theory and Applications Published by John Wiley & Sons Ltd.

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KEY WORDS: Colpitts; inductive degeneration; noise filter; optimum current density; oscillator analysis

1. INTRODUCTION

Modern wireless and wireline data communication systems impose severe requirements on phase noise (PN) at a given frequency offset from the carrier [1–3]. Accurate analysis of the behavior of oscillators has been the subject of intense investigation [4–8]. An effective method for providing qualitative and quantitative predictions of PN in integrated oscillators is based on the impulse sensitivity function (ISF) [9]. In [10, 11], the authors addressed how to derive accurate evaluations of the ISF in relation to simulation settings. Moreover, the authors in [10, 11] report topological investigations carried out for oscillation frequencies between 1 and 100 GHz, under the same design conditions in a 28-nm complementary metal-oxide semiconductor (CMOS) technology, taking into account both flicker and thermal noise contributions. The results showed for the first time that there is no best topology in the absolute sense as it may have appeared from previous studies reported in the literature limited to oscillators operating at a few gigahertz, but the opportunity of identifying the topology exhibiting the lowest PN depends also on the operating frequency range. Moreover, the use of the ISF allowed the separation of the total PN in its two components because of flicker and thermal noise from each

*Correspondence to: Domenico Zito, Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland.
†E-mail: domenico.zito@tyndall.ie

device in the oscillator circuit. In particular, it was observed how the tail transistor plays a significant role in the PN degradation occurring in the Colpitts oscillator circuit topology, here shown in Figure 1. In detail, the results in [11] show that minimizing the flicker noise in the output spectrum is particularly important because the $1/f^3$ PN region of integrated CMOS oscillators usually extends beyond 1 MHz offset from the oscillation frequency as a consequence of the deep sub-micrometer devices featuring $1/f$ corner frequencies of several tens or hundreds of megahertz. On the basis of these results, it is worth exploring techniques that allow reduction of PN, in particular due to the tail transistor.

An effective technique for the reduction of PN due to the tail transistor in CMOS LC oscillators was proposed in [12, 13]. Namely, the inductive degeneration of the tail transistor, which consists of introducing a high value off-chip inductance as a degeneration impedance to the source node of the tail transistor in a common-source cross-coupled differential pair oscillator circuit topology, in the specific case equal to 100 μH for an oscillator circuit operating around 2 GHz and implemented in 0.35-μm CMOS technology.

Moreover, the technique of noise filter was proposed in [14–16] for the reduction of PN due to the tail transistor in CMOS LC oscillators. In particular, it was capable to reduce the up-conversion of low-frequency noise. It consists of replacing the tail transistor with a band-stop filter, referred therein [14–16] as noise filter, in a common-source cross-coupled differential pair oscillator operating close to 1.1 GHz and fabricated in 0.35-μm CMOS technology.

These techniques for the reduction of PN due to the tail transistor are here applied to the Colpitts oscillator circuit topology of Figure 1. In particular, these techniques will be adopted and analyzed for a single-ended Colpitts topology designed in a 28-nm bulk CMOS process.

Our analyses will allow us to show mathematically and prove by means of simulations that there is a specific degeneration inductance value for M_2 in Figure 1, for which the PN of the Colpitts oscillator reaches a minimum. Furthermore, that there is a specific inductance value that tunes the resonance frequency of the noise filter to the oscillation frequency and for which the PN reaches a minimum, confirming the discussion in [14]. The analyses will allow also the evaluations about the dependence of the oscillation frequency on the degeneration inductance and filter components.

Moreover, a third technique for PN reduction, namely, optimum current density, will be proposed and analyzed in detail. It consists of biasing an oscillator circuit topology with the optimum bias current density for minimum PN. This technique of the optimum bias current density applied to specific metrics of interest has been extensively used for the design of low-noise amplifiers with minimum noise figure and the design of power amplifiers with a maximum linearity range [17, 18]. In a few cases, it has been also mentioned in achieving low PN in differential Colpitts and common-source cross-coupled differential pair oscillators [19–21]. Here, it will be applied to a single-ended

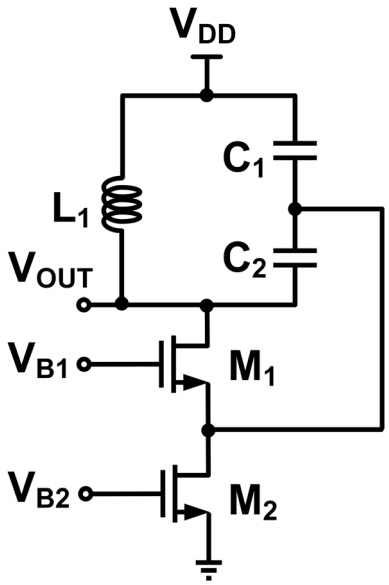

Figure 1. Single-ended Colpitts oscillator circuit topology. V_{B1} and V_{B2} are dc bias voltages.

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Colpitts oscillator circuit topology with the objective of providing adequate theoretical proofs of the benefits for its extensive use in oscillators. Our analyses will allow for the first time to gain insight into the theoretical details of this technique and its effective application, in addition to the oscillator performance optimization with respect to transconductance-to-current ratio (g_m/I_D); for example, [22].

Overall, the primary objective of this study reported here is to analyze by circuit theory and verify by circuit simulations, compare the results, and highlight the benefits emerging from the aforementioned PN reduction techniques applied to the Colpitts oscillator circuit topology. In particular, in our theoretical analyses, we will consider the equivalent circuit of the transistors with the typical parameters of a typical 28-nm bulk CMOS technology commercially available. The details of the equivalent circuits will be given in the related sections. The circuit simulations will be carried out within the Cadence design environment, which takes into account the full models of the transistors of a process design kit commercially available, including all their non-idealities and parasitic components. In our analyses, we will exclude the effects of the layout interconnections, because the additional parasitic components introduced by the layout could mask the results of the topological properties that we would like to bring to the light. Moreover, the exclusion of the effects of the layout interconnections is compliant with the expectations from theoretical analyses, because the additional parasitic components introduced by the layout would lead to cumbersome expressions that could limit the understanding of the results and opportunities to identify useful insights. Capacitors will be considered as ideal components, whereas a typical quality factor (Q) of 10 will be considered for all the spiral inductors [23]. Because the quality factor of the LC tank has a heavy impact on the PN, this condition will assure that all the oscillator circuits will be compared under common conditions [24–26]. All the transistors have minimum length. The reference values of the circuit components used for the theoretical analyses and circuit simulations are reported in Appendix. PN circuit simulations are carried out by means periodic steady state and periodic noise analyses in SpectreRF simulator. Details on simulation settings for accurate results can be found in [10, 11].

The paper is organized as follows. Section 2 addresses the inductive degeneration of the tail current transistor in a Colpitts oscillator. The analytical expressions of the oscillation frequency and the optimum inductance are derived by means of circuit theory and validated by means of the results provided by SpectreRF simulations in Cadence. Section 3 addresses the noise filter technique where the tail current transistor is replaced by a passive band-stop filter, that is, noise filter. The analytical expressions of the oscillation frequency and the optimum inductance are also derived by means of circuit theory and compared with the results obtained by means of SpectreRF simulations. Section 4 addresses the optimum current density for minimum PN for the Colpitts oscillator circuit topology under examination. The theoretical results are validated by the results obtained from SpectreRF simulations for oscillation frequency of 10 GHz. Finally, conclusions are drawn in Section 5.

2. INDUCTIVE DEGENERATION

In this section, we will derive an analytical expression for the oscillation frequency (f_0) of the Colpitts oscillator circuit topology in which we introduced an inductive degeneration (L_2) to the source node of the tail current transistor (M_2), as shown in Figure 2(a).

In order to extract appropriate evaluations about the improvement of performance with respect to the traditional topology of Figure 1, the oscillator circuit design will be carried out under the same transistor size, power and current consumptions, and inductance of the tanks and their quality factors, as in [10, 11]. Specifically, the transistor width is 30 μm, whereas the power consumed is 6.3 mW. V_{DD} is equal to 1 V. The tank inductance is equal to 500 pH.

2.1. Oscillation frequency

The Colpitts oscillator circuit topology with an inductively degenerated tail current transistor (M_2) is shown in Figure 2(a). Its small-signal equivalent circuit is shown in Figure 2(b). This equivalent circuit is obtained by considering the simplified transistor model with the small-signal

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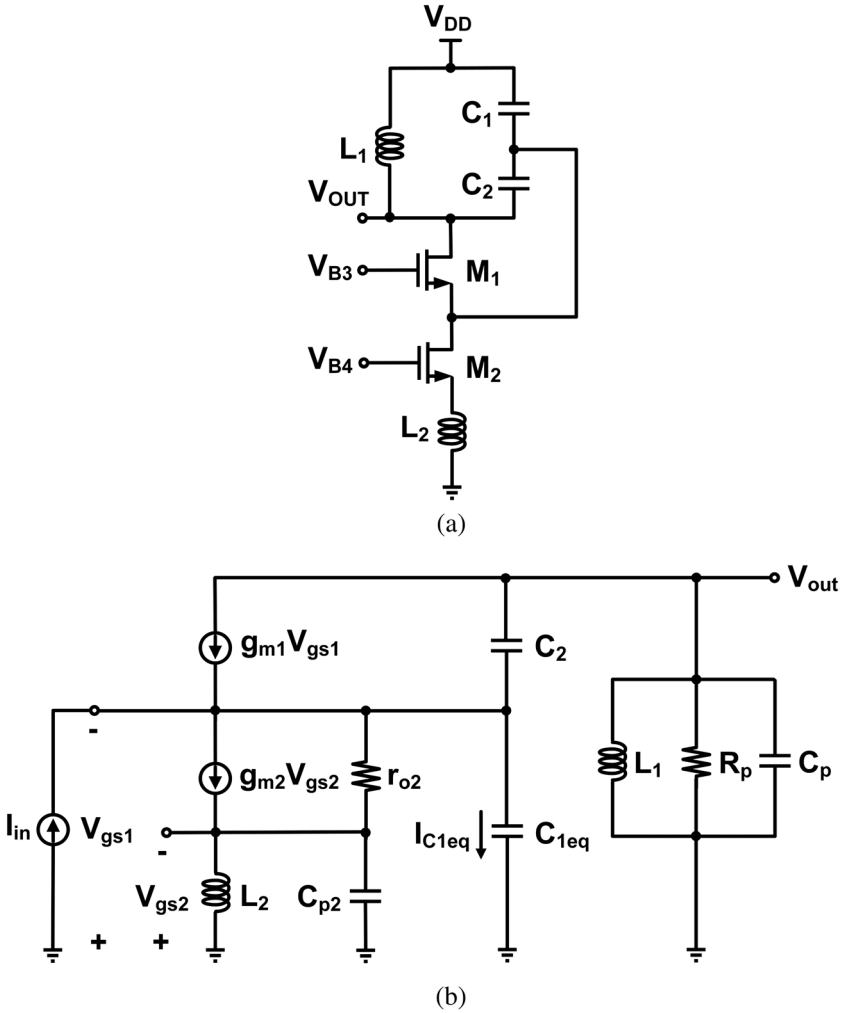

Figure 2. (a) Colpitts oscillator circuit topology incorporating an inductive degeneration (L_2) to the source node of the tail current transistor (M_2). V_{B3} and V_{B4} are dc bias voltages. (b) Small-signal equivalent circuit. I_{in} is the input current stimulus used for the calculation of the closed-loop gain V_{out}/I_{in}.

transconductance (g_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), source-to-bulk capacitance (C_{sb}), drain-to-bulk capacitance (C_{db}), and output resistance (r_{o2}). In the interest of a low complexity of the derived equations, the small-signal output resistance r_{o1} of M_1 as well as the polysilicon gate resistance r_g of M_1 and M_2 are neglected. Later, we will see that this working hypothesis is acceptable. If the small-signal output resistance r_{o2} of M_2 is also neglected, it can be proved that the oscillation frequency f_0 does not depend on L_2. Thereby, in order to take into account the effect of L_2 in f_0, r_{o2} is considered in the equivalent circuit. R_p represents the total load resistance of the LC tank, including the effect of the finite Q and the resistance seen from the source of M_1 scaled by the capacitive divide factor. C_p is the parasitic capacitance at the drain node of M_1, equal to the sum of C_{db1} and C_{gd1}. C_{p2} is the parasitic capacitance at the source node of M_2, equal to the sum of C_{gs2} and C_{sb2}. C_1 appears in parallel with C_{gs1}, C_{sb1}, C_{gd2}, and C_{db2}. Their sum can be represented as an equivalent capacitance C_{1eq}.

In order to excite the circuit into oscillation, we insert a current stimulus I_{in} at the source of M_1. We can now write that

$$C_p = C_{db1} + C_{gd1} \tag{1}$$

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$$C_{p2} = C_{gs2} + C_{sb2} \tag{2}$$

$$C_{1eq} = C_1 + C_{gs1} + C_{sb1} + C_{gd2} + C_{db2} \tag{3}$$

From Kirchhoff current law (KCL) at the source of M_2 it derives that

$$g_{m2}V_{gs2} + \frac{-V_{gs1} + V_{gs2}}{r_{o2}} + \frac{V_{gs2}}{sL_2} + V_{gs2}sC_{p2} = 0 \tag{4}$$

By applying the KCL at the source of M_1 and the output node, we can write

$$g_{m2}V_{gs2} - I_{in} + \frac{-V_{gs1} + V_{gs2}}{r_{o2}} + I_{C_{1eq}} + \frac{V_{out}}{sL_1} + \frac{V_{out}}{R_p} + V_{out}sC_p = 0 \tag{5}$$

Solving (4) with respect to V_{gs2} and combining with (5), we obtain

$$I_{C_{1eq}} = I_{in} - \left[\frac{1}{g_{m2} + \frac{1}{r_{o2}} + \frac{1}{sL_2} + sC_{p2}}\frac{1}{r_{o2}}\left(g_{m2} + \frac{1}{r_{o2}}\right) - \frac{1}{r_{o2}}\right] \times V_{gs1} - \left(\frac{1}{sL_1} + \frac{1}{R_p} + sC_p\right)V_{out} \tag{6}$$

Additionally, V_{gs1} is given by

$$V_{gs1} = -I_{C_{1eq}}\frac{1}{sC_{1eq}} \tag{7}$$

Moreover, from KCL at the output node,

$$g_{m1}V_{gs1} + \left(V_{out} + V_{gs1}\right)sC_2 + \frac{V_{out}}{sL_1} + \frac{V_{out}}{R_p} + V_{out}sC_p = 0 \tag{8}$$

which can be expressed as a function of V_{gs1} as follows

$$V_{gs1} = -\frac{1}{g_{m1} + sC_2}\left(sC_2 + \frac{1}{sL_1} + \frac{1}{R_p} + sC_p\right)V_{out} \tag{9}$$

Using (6) in (7), expressing the result as a function of V_{gs1} and equating to (9), we can express the closed-loop transfer function V_{out}/I_{in} as a ratio. By equating the imaginary part of the denominator of V_{out}/I_{in} to zero, we find that the oscillation frequency is given by (10)–(13). To reduce the complexity of the expression, C_{p2} is neglected in the equation for f_0 reported hereinafter.

$$f_o = \frac{1}{2\pi}\omega_0 \tag{10}$$

$$\omega_o = \sqrt{\frac{N_1}{D_1}} \tag{11}$$

where

$$N_1 = \left(L_1 g_{m1} + C_{1eq}R_p + C_2R_p + L_2R_p g_{m1}g_{m2}\right)r_{o2} + L_1 + L_2R_p g_{m1} \tag{12}$$

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$$D_1 = \left(C_{1eq}C_2R_p + C_{1eq}C_pR_p + C_2C_pR_p + C_{1eq}L_2g_{m2} + C_2L_2g_{m2} + C_pL_2R_pg_{m1}g_{m2}\right)L_1r_{o2} + \left(C_{1eq} + C_2 + C_pR_pg_{m1}\right)L_1L_2 \quad (13)$$

Figure 3 shows the results obtained by theoretical expressions of the oscillation frequency provided by (10)–(13), as a function of the LC tank capacitance C_{tank} expressed as

$$C_{tank} = \frac{C_{1eq}C_2}{C_{1eq} + C_2} + C_p \quad (14)$$

The simulations are repeated for three values of L_2 in order to demonstrate the weak dependence of the oscillation frequency f_0 on L_2. This means that L_2 can be sized to satisfy other design requirements, with limited effects on the oscillation frequency. This result will be exploited in the next section. Moreover, note that the oscillation frequency predicted by (10)–(13) closely follows the simulation results obtained by SpectreRF. In particular, the maximum difference amounts to about 50 MHz, observed for $L_2 = 2$ nH. Thereby, the aforementioned simplifications in the derivation of (10)–(13) are justified for an accurate first-order prediction of the oscillation frequency f_0.

2.2. *Optimum inductance for minimum phase noise*

Here, our aim is to explore the dependence of PN on L_2 and to derive under which condition the PN in the output spectrum of the Colpitts oscillator circuit topology of Figure 2(a) could be minimized. The theoretical results will be compared with respect to the simulation results obtained by means of SpectreRF.

From [27], we can write

$$V_1 = I_1\frac{R_pn}{n^2G_{m1}R_p + 1} \quad (15)$$

$$V_1 = I_1R_p(1 - n)n \quad (16)$$

$$V_{tank} = \frac{V_1}{n} \quad (17)$$

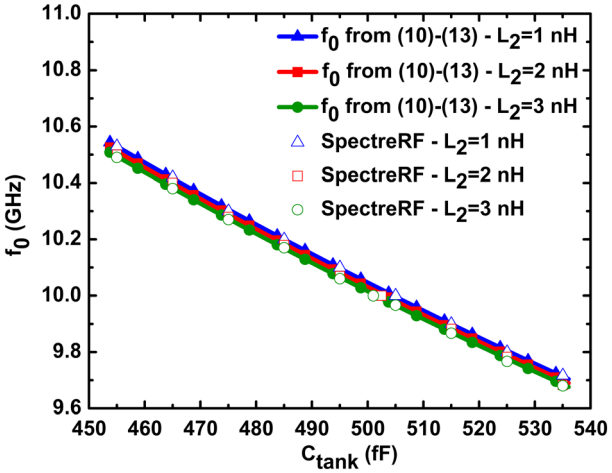

Figure 3. Oscillation frequency values versus C_{tank} for the circuit of Figure 2(a), predicted by (10)–(13) and simulated in SpectreRF for an oscillation frequency in the vicinity of 10 GHz.

DOI: 10.1002/cta

where V_1 and I_1 are the amplitudes of the fundamental harmonics of the source voltage and drain current of M_1, respectively. V_{tank} is the amplitude of the fundamental harmonic of the tank voltage. G_{m1} is the large-signal transconductance of M_1, and n is the capacitive divide factor equal to $C_2/(C_{1eq}+C_2)$.

The power spectral density of the flicker noise current of M_1 can be written as follows [28]:

$$\frac{\overline{i_d^2}}{\Delta f} = \frac{K g_{m1}^2}{2\left(\mu_n C_{ox}\frac{W}{L}\right) C_{ox} L^2 f} \tag{18}$$

where K is a process dependent parameter, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of M_1, respectively, and f is the frequency.

Moreover, the small-signal transconductance g_{m1} of M_1 and the PN for the Colpitts oscillator due to flicker noise from M_1 can be expressed as [29–32]

$$g_{m1} = \left(\mu_n C_{ox}\frac{W}{L}\right) V_1 (cos\ \phi - \cos\ \Phi) \tag{19}$$

$$\mathscr{L}(\Delta\omega)|_{flicker} = N\frac{1}{2q_{\max}^2 \Delta\omega^2} \Gamma_{id,dc}^2 \frac{\overline{i'^2_d}}{\Delta f} \tag{20}$$

where ϕ is equal to $\omega_0 t$ and Φ is half the conduction angle defined by

$$\Phi = cos^{-1}\left(\frac{V_{GS}-V_T}{V_1}\right) \tag{21}$$

with V_{GS} and V_T being the direct current (dc) gate-to-source voltage and the threshold voltage of M_1, respectively. Moreover, $N=1$ for the single-ended Colpitts, $q_{\max}$ is the maximum charge displacement across the tank capacitance, $\Delta\omega$ is the angular frequency offset from the oscillation frequency, $\frac{\overline{i'^2_d}}{\Delta f}$ is equal to $\frac{\overline{i_d^2}}{\Delta f} \times \frac{1}{cos\ \phi - cos\ \Phi}$, and $\Gamma_{id,dc}^2$ is the square dc value of the ISF given by [30–32]

$$\Gamma_{id,dc}^2 = \frac{\omega_{1/f^3}}{\omega_{1/f}} \Gamma_{id,rms}^2 \tag{22}$$

where $\Gamma_{id,rms}^2$ can be derived from [29]

$$\Gamma_{id,rms}^2 = \frac{1}{2\pi}\frac{(1-n)^2}{N^2}\left[\Phi - \frac{1}{2}sin(\Phi)\right] \tag{23}$$

Thereby, (20) now becomes

$$\mathscr{L}(\Delta\omega)|_{flicker} = N\frac{1}{2q_{max}^2 \Delta\omega^2}\frac{\omega_{1/f^3}}{\omega_{1/f}} \Gamma_{id,rms}^2 \frac{\overline{i'^2_d}}{\Delta f} \tag{24}$$

In order to take into account the cyclostationarity of the noise from M_1, we replace $\Gamma_{id,rms}^2$ in (24) with $\Gamma_{id,eff,rms}^2$, that is, the square root mean square value of the effective ISF [8,29]

$$\Gamma_{id,eff,rms}^2 = \frac{(1-n)^2}{N^2}\frac{I_1}{2\left(\mu_n C_{ox}\frac{W}{L}\right) V_1^2} \tag{25}$$

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Combining (18) and (19), the flicker noise current can be rewritten as follows

$$\frac{\overline{i_d^2}}{\Delta f} = \frac{K\left(\mu_n C_{ox}\frac{W}{L}\right)}{2C_{ox}L^2 f} V_1^2 (cos\ \phi - \cos\ \Phi)^2 = \frac{\overline{i'^2_d}}{\Delta f}(cos\ \phi - \cos\ \Phi)^2 \tag{26}$$

Thereby, using (26) into (24), we yield

$$\mathscr{L}(\Delta\omega)|_{flicker} = N\frac{1}{2q_{max}^2\Delta\omega^2}\frac{\omega_{1/f^3}}{\omega_{1/f}}\Gamma^2_{id,eff,rms}\frac{\overline{i_d^2}}{\Delta f}\frac{1}{(cos\ \phi - cos\ \Phi)^2} \tag{27}$$

Then we substitute $\frac{\overline{i_d^2}}{\Delta f}$ and $\Gamma^2_{id,eff,rms}$ in (27) as expressed by (18) and (25), respectively. Rearranging the result by using (15)–(17), we arrive in the following expression

$$\mathscr{L}(\Delta\omega)|_{flicker} = \left|\frac{\pi(1-n)^2 K}{4N}\frac{\omega_{1/f^3}}{\omega_{1/f}}\frac{n^2 G_{m1}R_p + 1}{V_{tank}R_p C_{tank}^2\Delta\omega^3 C_{ox}L^2}\right| \tag{28}$$

In order to excite the Colpitts oscillator circuit topology of Figure 2(a), a stimulus can be applied to different nodes. The type of stimulus (voltage or current) must be chosen such that when it is set to zero, the circuit returns to its original topology [33]. The large-signal equivalent circuit of the Colpitts oscillator topology of Figure 2(a) is shown in Figure 4.

V_{in} is a voltage stimulus applied to the gate of M_1. Transistor M_1 is represented as a transconductance amplifier according to the describing function analysis [27]. G_{m1} is the large-signal transconductance of M_1, equal to the ratio of the fundamental harmonic of the drain current of M_1 to the fundamental harmonic of the gate-source voltage of M_1. For transistor M_2, a simplified large-signal equivalent circuit is used [34, 35]. This equivalent circuit is obtained by considering the simplified transistor model with the large-signal transconductance (G_m), gate-to-source capacitance (C_{GS}), gate-to-drain capacitance (C_{GD}), source-to-bulk capacitance (C_{SB}), drain-to-bulk capacitance (C_{DB}), and output resistance (R_{DS}). G_{m2} is approximated by the average value of g_{m2} during the oscillation period. C_1 appears in parallel with C_{GD2} and C_{DB2}. Their sum can be represented as an equivalent large-signal capacitance C_{1EQ}. C_{P2} is the parasitic capacitance at the source node of M_2, equal to the sum of C_{GS2} and C_{SB2}. R_{DS2} is approximated by the average value of r_{o2} during the

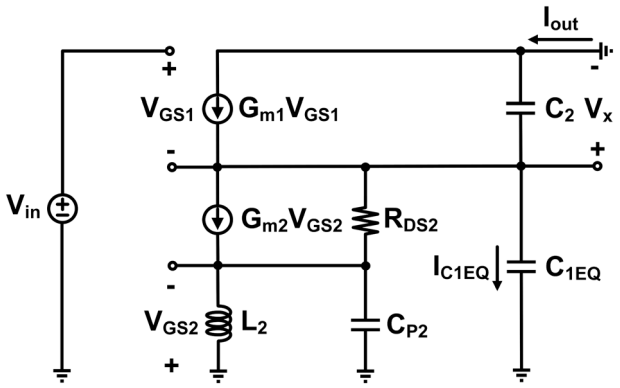

Figure 4. Large-signal equivalent circuit of the Colpitts oscillator circuit topology of Figure 2(a). G_{m1} and G_{m2} are the large-signal transconductance of M_1 and M_2, respectively. V_{in} is a voltage stimulus applied to the gate of M_1.

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oscillation period. For simplicity of our analysis, it is assumed that, at the oscillation frequency of 10 GHz, extrinsic components as well as the gate and substrate resistances have a negligible effect to PN [36, 37]. Later, we will verify that this assumption is acceptable.

We can now write

$$C_{1EQ} = C_1 + C_{GD2} + C_{DB2} \tag{29}$$

$$C_{P2} = C_{GS2} + C_{SB2} \tag{30}$$

We will now calculate the equivalent transconductance for the circuit of Figure 4 with respect to the voltage stimulus V_{in}, that is, $G_{m,eq1} = I_{out}/V_{in}$. Next, we will determine L_2 for which the flicker and thermal PN components at the output of the Colpitts oscillator circuit topology of Figure 2(a) reach the minimum values. For simplicity of the derived equations, C_{P2} will be neglected.

From Kirchhoff voltage law

$$V_{GS1} = V_{in} - V_x \tag{31}$$

then from KCL at the source of M_2

$$I_{C_{1EQ}} - \frac{V_{GS2}}{sL_2} - I_{out} = 0 \tag{32}$$

which can be rewritten as

$$V_{GS2} = -I_{out} sL_2 + V_x s^2 L_2 C_{1EQ} \tag{33}$$

Moreover, from KCL at the source of M_1,

$$V_x sC_2 - G_{m1} V_{GS1} + G_{m2} V_{GS2} + V_x sC_{1EQ} + \frac{V_x + V_{GS2}}{R_{DS2}} = 0 \tag{34}$$

Finally, from KCL at the drain of M_1,

$$G_{m1} V_{GS1} - I_{out} - V_x sC_2 = 0 \tag{35}$$

Furthermore, we can substitute V_{GS1} in (35) with its value given by (31). Using (31) and (33) into (34), solving with respect to V_x and substituting for V_x in (35), $G_{m,eq1}$ can be written as

$$G_{m,eq1} = \frac{N_2}{D_2} \tag{36}$$

$$N_2 = G_{m1}(C_{1EQ}L_2 + C_{1EQ}L_2 G_{m2} R_{DS2}) s^2 + C_{1EQ} G_{m1} R_{DS2} s + G_{m1} \tag{37}$$

$$\begin{aligned} D_2 = {} & (C_{1EQ}L_2 + C_2 L_2 + C_{1EQ}L_2 G_{m2} R_{DS2} + C_2 L_2 G_{m2} R_{DS2}) s^2 \\ & + (L_2 G_{m1} + C_{1EQ} R_{DS2} + C_2 R_{DS2} + L_2 G_{m1} G_{m2} R_{DS2}) s + G_{m1} R_{DS2} + 1 \end{aligned} \tag{38}$$

By replacing G_{m1} with $G_{m,eq1}$ in (28), taking the derivative with respect to L_2 and equating to zero, we find the value of L_2 for which the flicker noise present at the output of the Colpitts oscillator circuit topology of Figure 2(a) reaches a minimum, that is,

DOI: 10.1002/cta

$$L_2 = \left|\frac{N_3}{D_3}\right| \tag{39}$$

where

$$N_3 = \left(-C_{1EQ}R_pG_{m1}R_{DS2}n^2 - C_{1EQ}R_{DS2} - C_2R_{DS2}\right)s - R_pG_{m1}n^2 - G_{m1}R_{DS2} - 1 \tag{40}$$

$$\begin{aligned} D_3 = \big(&C_{1EQ} + C_2 + C_{1EQ}G_{m2}R_{DS2} + C_2G_{m2}R_{DS2} + C_{1EQ}R_pG_{m1}n^2 \\ &+C_{1EQ}R_pG_{m1}G_{m2}n^2R_{DS2}\big)s^2 + (G_{m1} + G_{m1}G_{m2}R_{DS2})s \end{aligned} \tag{41}$$

A similar derivation can also be performed for the PN component because of the thermal noise of M_1, M_2, L_2, and the LC tank. From [27,29], we have

$$G_{m1} = \frac{-I_1}{V_1} \tag{42}$$

$$I_1 = 2I_B\left(1 - \frac{\Phi^2}{14}\right) \tag{43}$$

where

$$I_B = \frac{\left(\mu_nC_{ox}\frac{W}{L}\right)V_1^2}{15\pi}\Phi^5\left(1 - \frac{4}{21}\Phi^2\right) \tag{44}$$

The PN expression due to the thermal noise is

$$\mathscr{L}(\Delta\omega)|_{thermal} = \left|\frac{K_BT}{4NI_B^2R_p^3C_{tank}^2\Delta\omega^2}\left(1 - \frac{\Phi^2}{14}\right)^{-2} \times \left(\frac{\gamma}{n(1-n)} + \frac{1}{(1-n)^2} + \frac{n^2R_p\gamma G_{m2}}{(1-n)^2}\right)\right| \tag{45}$$

where $K_B = 1.38 \times 10^{-23}\, V \times C/K$ is the Boltzmann constant and T is the absolute temperature.

Combining (42) and (43), we obtain

$$V_1 = -\frac{1}{G_{m1}}2I_B\left(1 - \frac{\Phi^2}{14}\right) \tag{46}$$

Moreover, (44) can be rewritten as

$$V_1 = \left|\frac{15\pi}{\left(\mu_nC_{ox}\frac{W}{L}\right)}I_B\Phi^{-5}\left(1 - \frac{4}{21}\Phi^2\right)^{-1}\right|^{1/2} \tag{47}$$

Taking the absolute value of (46), equating to (47), and then solving with respect to I_B

$$I_B = \frac{15\pi}{\left(\mu_nC_{ox}\frac{W}{L}\right)}\frac{1}{4}G_{m1}^2\left(1 - \frac{\Phi^2}{14}\right)^{-2}\Phi^{-5}\left(1 - \frac{4}{21}\Phi^2\right)^{-1} \tag{48}$$

Afterwards, we substitute G_{m1} in (48) with the expression of $G_{m,eq1}$ given by (36)–(38) and then use the calculated value of I_B in (45). After taking the derivative of the resulting equation with respect to L_2

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and equate to zero, we find that the value of L_2, for which the thermal noise at the output of the Colpitts oscillator circuit topology of Figure 2(a) reaches a minimum, is

$$L_2 = \left|\frac{N_4}{D_4}\right| \tag{49}$$

where

$$N_4 = (-C_{1EQ}R_{DS2} - C_2R_{DS2})s - G_{m1}R_{DS2} - 1 \tag{50}$$

$$D_4 = (C_{1EQ} + C_2 + C_{1EQ}G_{m2}R_{DS2} + C_2G_{m2}R_{DS2})s^2 + (G_{m1} + G_{m1}G_{m2}R_{DS2})s \tag{51}$$

The total PN expression is found by adding the flicker and thermal PN components given by (28) and (45), respectively, as follows:

$$\mathscr{L}(\Delta\omega)|_{total} = 10log_{10}\left[\mathscr{L}(\Delta\omega)|_{flicker} + \mathscr{L}(\Delta\omega)|_{thermal}\right] \tag{52}$$

The total PN given by (52) is plotted in Figure 5 versus L_2, at an average bias current of 6.3 mA, for an oscillation frequency of 10 GHz, at a 1-MHz frequency offset. C_1 and C_2 have equal size, and their value changes according to the value of L_2, keeping f_0 constant at 10 GHz. Moreover, V_{B3} and V_{B4} are chosen to have the same average current, also considering the voltage drop across the parasitic resistance of L_2. Note the agreement between the theoretical derivations and the SpectreRF simulations. In particular, the maximum difference between the results of the theoretical derivations and circuit simulations is about 2 dB.

Thereby, the aforementioned simplifications in the derivation of (39)–(41) and (49)–(51) are acceptable for a first order and lead to a relatively accurate derivation of the optimum inductance value (L_2) for which the Colpitts oscillator circuit topology of Figure 2(a) exhibits a minimum PN.

From SpectreRF simulations, for an oscillation frequency of 10 GHz, a minimum PN is achieved for L_2 equal to about 4 nH. This value of inductance can be obtained by means of integrated inductors.

The existence of an optimum value for L_2 for minimum noise contribution from M_2 can be explained as follows. Assuming that the tail transistor M_2 generates a flicker and thermal noise current with power equal to $\overline{I_n^2}$, then the power of the noise current at the drain of M_2, $\overline{I_{n,out}^2}$, is equal to $\overline{I_n^2}/(Z_S g_{m2} + 1)^2$,

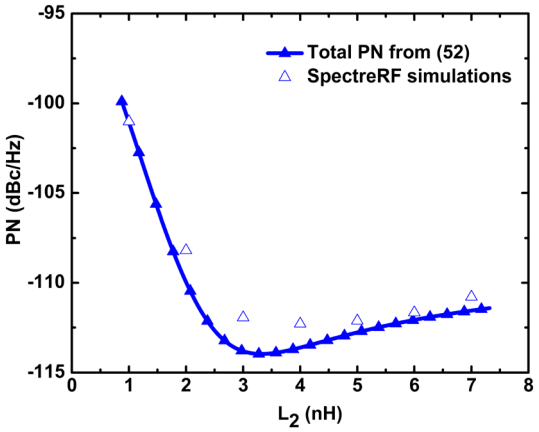

Figure 5. Total PN at a 1-MHz frequency offset from the carrier versus the degeneration inductance L_2 at an average bias current of 6.3 mA, for the circuit of Figure 2(a), predicted by (52) and obtained by SpectreRF simulations for an oscillation frequency of 10 GHz.

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where Z_S is the impedance of the parallel combination of L_2 with the capacitance present at the source node of M_2, which is C_{p2} shown in Figure 2(b).

$\overline{I_{n,out}^2}$ versus frequency is plotted in Figure 6. R_{p2} is the parallel resistance representing the losses of L_2. It can be observed that $\overline{I_{n,out}^2}$ shows a minimum at the resonance frequency of the bandpass filter formed by L_2 and C_{p2}. At that frequency, Z_S takes its maximum value, which means that the impedance Z_{out} looking down from the drain of M_2 and equal to $[1+(g_{m2}+g_{mb2})r_{o2}]Z_S+r_{o2}$ will also be maximized. According to the authors in [14, 15], for single-ended Colpitts, the impedance (magnitude) seen at the source of M_1 should be maximum at the oscillation frequency of the oscillator topology. Thereby, in order to have the maximum value of Z_{out} at the oscillation frequency, the resonance frequency f_{filter} of the bandpass filter at the source of M_2 should be equal to the oscillation frequency.

In regard of the up-conversion of the flicker noise from M_1 and M_2, it is reduced as follows. The inductive degeneration acts in a similar way to the noise filter, because at f_{filter}, the nonlinear capacitance at the source node of M_2 is cancelled by L_2. Thereby, the modulation of the current flowing through the nonlinear junction capacitance at the source node of M_2 and then through M_1 to the output is minimized.

At this stage, it is worth also comparing these results obtained from the Colpitts topology with the inductive degeneration with those obtained for the traditional Colpitts oscillator circuit topology of Figure 1, previously reported in [11]. In particular, from [11], the PN obtained under the same design conditions amounts to −96.25 dBc/Hz for an oscillation frequency of 10 GHz. Comparing this PN performance with the results obtained here and reported in Figure 5, we can observe that the Colpitts topology with inductive degeneration can lead potentially to a PN reduction up to 16 dB.

Last, the results presented in [10, 11] show that the $1/f^3$ region of the PN extends above a 1-MHz frequency offset for the Colpitts oscillator topology under study. This is a consequence of the adoption of nanoscale CMOS technologies characterized by flicker noise corners of several tens or hundreds of megahertz, which lead to flicker noise up-conversion being responsible for most of PN [38] even at large offsets from the carrier frequency. Thereby, the optimum inductance value for the total PN shown in Figure 5 is very close to that given by (39)–(41), because at a 1-MHz offset, thermal noise has a negligible effect on PN.

3. NOISE FILTER

In this section, we will derive the analytical expression for the oscillation frequency (f_0) of a Colpitts oscillator circuit topology in which we introduced a band-stop filter (L_3, C_3) to the source node of M_1 as shown in Figure 7(a). Because of its noise filtering action, it is referred therein [14–16] as noise filter. Moreover, we will observe that there is an optimum inductance value (L_3) for which the oscillator circuit topology exhibits a minimum PN, and we will calculate such an optimum inductance that leads the noise filter to resonate at the oscillation frequency, as mentioned in Section 1. It is worth emphasizing that the circuit topology incorporating the noise filter, as in Figure 7(a), is different from the circuit topology with inductive degeneration, as in Figure 2(a). Thereby, despite the analyses reported in Section 1 and the analyses reported hereinafter share the

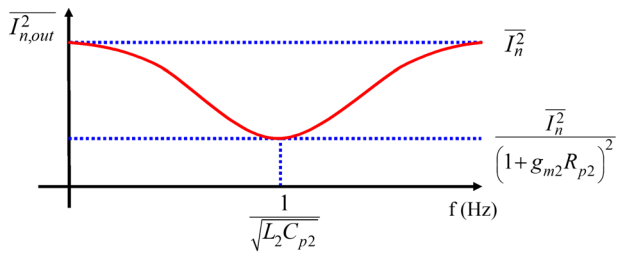

Figure 6. Power of the noise current at the drain of M_2 in Figure 2(a) versus frequency.

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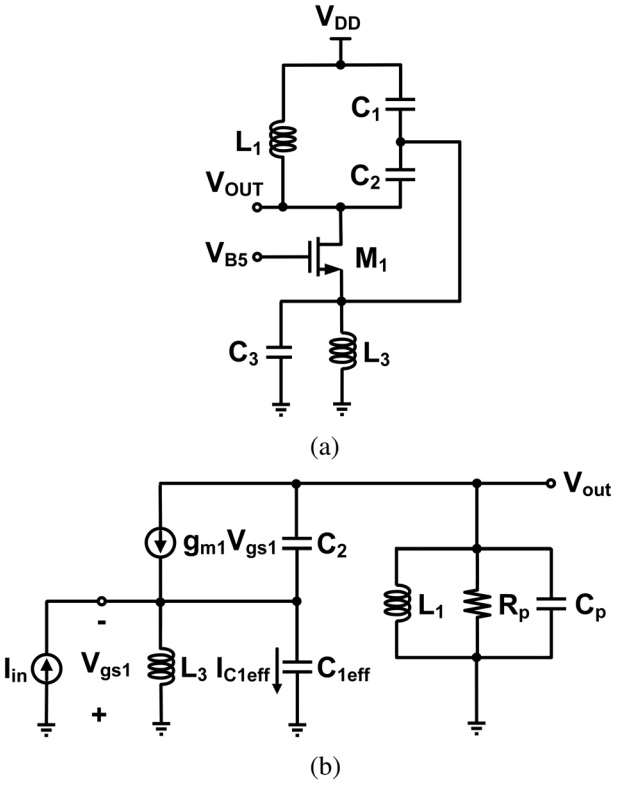

Figure 7. (a) Colpitts oscillator circuit topology incorporating a noise filter. V_{B5} is the dc bias voltage. (b) Small-signal equivalent circuit. I_{in} is the input current stimulus used for the calculation of the closed-loop gain V_{out}/I_{in}.

same objectives, they are different from each other because the two oscillator circuit topologies, one with inductive degeneration and one with noise filter, lead to different sets of equations in the two cases.

Again, in order to extract appropriate evaluations about the improvement of PN performance with respect to the traditional topology of Figure 1, the oscillator circuit design will be carried out under the same transistor size, power and current consumption, and inductance of the tank and its quality factor, as in [10, 11].

3.1. Oscillation frequency

The Colpitts oscillator circuit topology incorporating a noise filter is shown in Figure 7(a). Its small-signal equivalent circuit is shown in Figure 7(b). This equivalent circuit is obtained by considering the simplified transistor model with the small-signal transconductance (g_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), source-to-bulk capacitance (C_{sb}), and drain-to-bulk capacitance (C_{db}). To reduce the complexity of the derived equations, the small-signal output resistance r_{o1} as well as the polysilicon gate resistance r_g of M_1 are neglected. Later, we will verify that this hypothesis is acceptable. R_p represents the total load resistance of the LC tank, including the effect of the finite Q of the tank and the resistance seen from the source of M_1 scaled by the capacitive divide factor.

The junction capacitances of transistors M_1 and M_2 in Figure 1 behave nonlinearly during the oscillation period. One of the major up-conversion mechanisms of flicker noise is the modulation of the current flowing through the capacitance at the source node of M_1 [38]. By removing M_2, the modulation of the current flowing through this capacitance is significantly reduced, because of the decrease of the nonlinear parasitic capacitance.

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The presence of an optimum L_3 for minimum PN is due to the resonance with the capacitance at the source node of M_1, which exhibits ideally high impedance at the resonance frequency of the noise filter. This results in further decrease of the modulation current, because this capacitance is effectively tuned out by L_3.

C_3 can be varied in order to tune the oscillation frequency, avoiding changes in the tank capacitance. Moreover, the amplitude of the tank voltage can be larger than that in the topology of Figure 1, because there is no reduction of voltage headroom due to the tail transistor.

It is worth noting that because no varactor was used in the circuit of Figure 7(a), there are only two major up-conversion mechanisms: the modulation of the current flowing through the capacitance at the source node of M_1 and the modulation of the harmonic content of the output voltage waveform (i.e., Groszkowski effect). The adoption of the noise filter can minimize the first cause of flicker noise up-conversion [38].

C_{gs1}, C_{sb1} and C_3 appear in parallel with C_1, and their sum can be expressed as an effective capacitance

$$C_{1eff} = C_1 + C_{gs1} + C_{sb1} + C_3 \tag{53}$$

C_p is the parasitic capacitance present at the drain node of M_1, given by

$$C_p = C_{db1} + C_{gd1} \tag{54}$$

In order to excite the circuit into oscillation, we insert a current stimulus I_{in} at the source of M_1. From KCL at the source of M_1, we obtain

$$I_{C1eff} - I_{in} - \frac{V_{gs1}}{sL_3} + \frac{V_{out}}{sL_1} + \frac{V_{out}}{R_p} + V_{out}sC_p = 0 \tag{56}$$

and also

$$V_{gs1} = -I_{C1eff}\frac{1}{sC_{1eff}} \tag{57}$$

Solving (56) for I_{C1eff} and using the result in (57), we find

$$V_{gs1} = \frac{1}{1 + \frac{1}{s^2L_3C_{1eff}}}\frac{1}{sC_{1eff}}\left(-I_{in} + \frac{V_{out}}{sL_1} + \frac{V_{out}}{R_p} + V_{out}sC_p\right) \tag{58}$$

and from KCL at the output,

$$g_{m1}V_{gs1} + \left(V_{out} + V_{gs1}\right)sC_2 + \frac{V_{out}}{sL_1} + \frac{V_{out}}{R_p} + V_{out}sC_p = 0 \tag{59}$$

Expressing (59) as a function of V_{gs1} and equating to (58), we can derive the closed-loop transfer function V_{out}/I_{in} as a ratio. By equating the real part of the denominator of this ratio to zero, we find that the oscillation frequency is given by

$$f_o = \frac{1}{2\pi}\omega_0 \tag{60}$$

DOI: 10.1002/cta

$$\omega_o = \sqrt{\frac{N_5}{D_5}} \tag{61}$$

where

$$\begin{aligned} N_5 &= C_{1eff}L_3R_p + C_2L_3R_p + C_2L_1R_p + C_pL_1R_p + L_1L_3g_{m1} + \Big(C_{1eff}^2L_3^2R_p^2 + 2C_{1eff}C_2L_3^2R_p^2 - \\ &2C_{1eff}C_2L_1L_3R_p^2 - 2C_{1eff}C_pL_1L_3R_p^2 + 2C_{1eff}L_1L_3^2R_pg_{m1} + C_2^2L_3^2R_p^2 + 2C_2^2L_1L_3R_p^2 + C_2^2L_1^2R_p^2 - \\ &2C_2C_pL_1L_3R_p^2 + 2C_2C_pL_1^2R_p^2 + 2C_2L_1L_3^2R_pg_{m1} + 2C_2L_1^2L_3R_pg_{m1} + C_p^2L_1^2R_p^2 + 2C_pL_1^2L_3R_pg_{m1} + L_1^2L_3^2g_{m1}^2\Big)^{1/2} \\ &\approx C_{1eff}L_3R_p + C_2L_3R_p + C_2L_1R_p + C_pL_1R_p + \Big(C_{1eff}^2L_3^2R_p^2 + 2C_{1eff}C_2L_3^2R_p^2 - 2C_{1eff}C_2L_1L_3R_p^2 + C_2^2L_3^2R_p^2 + \\ &2C_2^2L_1L_3R_p^2 + C_2^2L_1^2R_p^2\Big)^{1/2} \end{aligned} \tag{62}$$

$$D_5 = 2L_1L_3R_p\big(C_{1eff}C_2 + C_{1eff}C_p + C_2C_p\big) \approx 2L_1L_3R_pC_{1eff}C_2 \tag{63}$$

Figure 8 shows the theoretical estimation of the oscillation frequency provided by (60)–(63), as a function of C_3. Simulations are repeated for three different values of L_3 in order to show the dependence of f_0 on L_3, which turns out being significant. Note that the oscillation frequency predicted by (60)–(63) closely follows the results obtained by circuit simulations. In particular, the maximum difference is about 70 MHz, observed for $L_3 = 2$ nH. Thereby, the aforementioned simplifications in the derivation of (60)–(63) are justified and lead to an accurate first-order prediction of the oscillation frequency f_0.

3.2. *Optimum inductance for minimum phase noise*

Here, the objective is to explore the dependence of PN on L_3 and to derive the condition for which the PN at the output of the Colpitts oscillator circuit topology of Figure 7(a) can be reduced. The theoretical results will be compared with those obtained by means of SpectreRF simulations.

The large-signal equivalent circuit of the Colpitts oscillator of Figure 7(a) is shown in Figure 9. V_{in} is a voltage stimulus applied to the gate of M_1. Transistor M_1 is represented by a transconductance amplifier according to the describing function analysis [27]. G_{m1} is the large-signal transconductance of M_1, equal to the ratio of the fundamental harmonic of the drain current of M_1 to the fundamental harmonic of the gate-source voltage of M_1.

G_{m1} does not take into account the degeneration effect because of the non-ideal bias provided by L_3. For this reason, first, we calculate the equivalent transconductance for the describing function model of

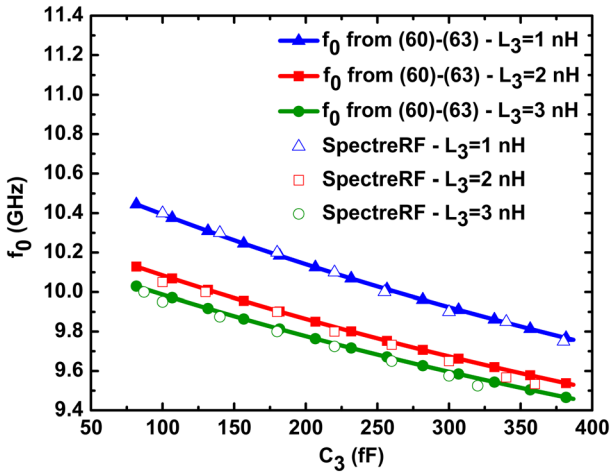

Figure 8. Oscillation frequency versus C_3 for the circuit of Figure 7(a) as predicted by (60)–(63) and SpectreRF simulations for an oscillation frequency in the vicinity of 10 GHz.

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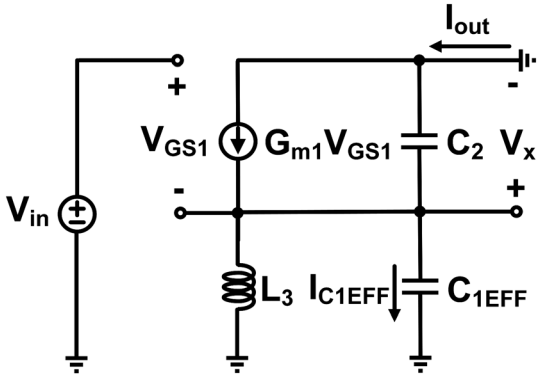

Figure 9. Large-signal equivalent circuit of the Colpitts oscillator circuit of Figure 7(a). G_{m1} is the large-signal transconductance of M_1. V_{in} is a voltage stimulus applied to the gate of M_1.

Figure 9 with respect to the voltage stimulus V_{in}, that is, $G_{m,eq2}=I_{out}/V_{in}$. Next, we will derive the condition on L_3 for which the flicker and thermal components of the PN at the output of the Colpitts oscillator circuit topology of Figure 7(a) can be minimized.

We can write

$$C_{1EFF} = C_1 + C_3 \tag{64}$$

$$Z_p = sL_3 // \frac{1}{sC_{1EFF}} = \frac{sL_3}{s^2L_3C_{1EFF}+1} \tag{65}$$

$$V_{in} = V_{GS1} + I_{out}Z_p \tag{66}$$

Using (65) into (66) and rewriting

$$V_{GS1} = V_{in} - I_{out}\frac{sL_3}{s^2L_3C_{1EFF}+1} \tag{67}$$

Moreover,

$$V_x = I_{out}Z_p = I_{out}\frac{sL_3}{s^2L_3C_{1EFF}+1} \tag{68}$$

From KCL at the drain of M_1, it derives

$$G_{m1}V_{GS1} - I_{out} - V_x sC_2 = 0 \tag{69}$$

Finally, replacing V_{GS1} and V_x into (69) with their values given by (67) and (68), respectively, we find $G_{m,eq2}$ as follows:

$$G_{m,eq2} = \frac{G_{m1}}{1 + G_{m1}\frac{sL_3}{s^2L_3C_{1EFF}+1} + \frac{s^2L_3C_2}{s^2L_3C_{1EFF}+1}} \tag{70}$$

By replacing G_{m1} in (28) with $G_{m,eq2}$ given by (70), taking the derivative with respect to L_3 and equating to zero, we find that the value of L_3 for which the flicker component of the PN at the output of the Colpitts oscillator circuit topology of Figure 7(a) reaches the minimum is given by

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$$L_3 = \left| \frac{R_p G_{m1} n^2 + 1}{\left(C_{1EFF} R_p G_{m1} n^2 + C_{1EFF} + C_2\right) s^2 + G_{m1} s} \right| \tag{71}$$

A similar derivation can also be performed for the PN component because of the thermal noise of M_1, L_3, and the LC tank. The PN expression due to the thermal noise is

$$\mathscr{L}(\Delta\omega)|_{thermal} = \left| \frac{K_B T}{4 N I_B^2 R_p^3 C_{tank}^2 \Delta\omega^2} \left(1 - \frac{\Phi^2}{14}\right)^{-2} \times \left(\frac{\gamma}{n(1-n)} + \frac{1}{(1-n)^2} + \frac{n^2 R_p}{(1-n)^2} \frac{1}{Q\omega L_3} \right) \right| \tag{72}$$

Then we substitute G_{m1} in (48) with the expression of $G_{m,eq2}$ given by (70) and use the calculated value of I_B in (72). After taking the derivative with respect to L_3 and equate to zero, we find that the value of L_3 for which the thermal PN component at the output of the Colpitts oscillator circuit topology of Figure 7(a) reaches the minimum is given by

$$L_3 = \left| \frac{1}{(C_{1EFF} + C_2) s^2 + G_{m1} s} \right| \tag{73}$$

The total PN is plotted in Figure 10 versus L_3, at an average current of 6.3 mA, for an oscillation frequency of 10 GHz, at a 1-MHz frequency offset. C_1 and C_2 have equal size, and their value changes according to the value of L_3, keeping f_0 constant at 10 GHz. C_3 is set equal to zero. Moreover, V_{B5} is chosen to have the same average current, also considering the voltage drop across the parasitic resistance of L_3. Note the relatively good agreement between the theoretical derivations and the SpectreRF simulations. In detail, the maximum difference between the results of the theoretical predictions and circuit simulations is about 1 dB.

From SpectreRF simulations, the minimum PN is achieved for L_3 approximately equal to 8 nH. Thereby, this result confirms the discussion in [15], according to which the optimum inductance value in terms of PN is expected to be the value that tunes the resonance frequency of the noise filter (L_3, C_3) to the oscillation frequency. This value of inductance can be obtained by means of integrated inductors.

At this stage, it is worth also comparing these results obtained from the Colpitts topology with noise filter of Figure 7(a) with those obtained for the traditional Colpitts oscillator circuit topology of

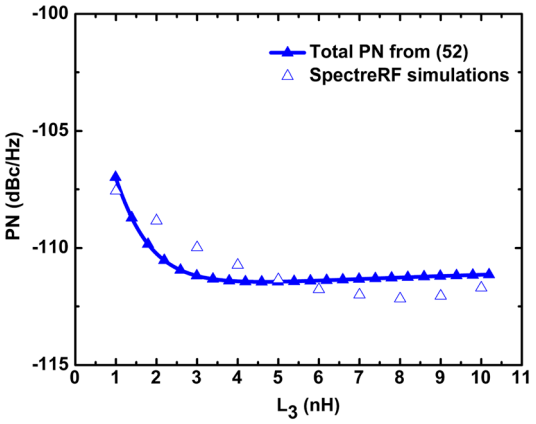

Figure 10. Total PN at a 1-MHz frequency offset from the carrier versus L_3, for the circuit of Figure 7(a) with an average bias current of 6.3 mA, as predicted by (52) and obtained by SpectreRF simulations for an oscillation frequency of 10 GHz.

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Figure 1, previously reported in [11]. In particular, from [11], the PN obtained under the same design conditions amounts to −96.25 dBc/Hz for an oscillation frequency of 10 GHz. Comparing such a PN performance with the results obtained here and reported in Figure 10, we can observe that the Colpitts oscillator circuit topology with noise filter can potentially allow a PN reduction up to 16 dB.

Last, coherently with the fact that the $1/f^3$ region of the PN extends beyond 1 MHz, as observed in [10, 11], we can also observe that the optimum inductance value for the total PN shown in Figure 10 is very close to that given by (71), because at a 1-MHz offset, thermal noise has a negligible effect.

4. OPTIMUM CURRENT DENSITY

In this section, we will examine the technique of biasing an oscillator topology with the optimum current density for the minimum PN. The effectiveness of this technique for oscillators was shown in [19–21] where the transistors were biased close to the current density per unit of width for minimum noise figure.

From the point of view of the PN analysis, an oscillator can be treated as a low-noise amplifier, needed to be noise matched to the signal source impedance, represented in this case by the tank impedance at the resonance frequency [18]. In low-noise amplifiers, the transistors should be biased with the optimum current density for minimum noise figure [17]. In oscillators, the quiescent point may vary significantly during the oscillation period, and thereby, the optimum current density for minimum PN may deviate from the dc bias current density for minimum noise figure of the transistors. Hence, in our analyses, we will consider the dc bias current (I_B) as the average total current. We will analyze and apply this third technique for further reduction of PN to the Colpitts oscillator topology incorporating either inductive degeneration or noise filter investigated earlier. Combining the benefits of this third technique with those of inductive degeneration or noise filter could lead to maximize the potential reduction of PN achievable for the oscillator circuit topology under common design conditions. First, in our analysis, the PN components due to flicker and thermal noise will be expressed as a function of the bias current. Next, the resulting equations will be plotted versus the bias current density and validated by means of the results provided by SpectreRF simulations in Cadence.

4.1. Inductive degeneration

Combining (17), (42), and (43), we yield

$$G_{m1} = -\frac{2I_B\left(1-\frac{\varphi^2}{14}\right)}{nV_{tank}} \tag{74}$$

With reference to the Colpitts oscillator circuit topology with the inductive degeneration (L_2) at the source node of the tail current transistor (M_2) shown in Figure 2(a), we use G_{m1} given by (74) into (36)–(38) in order to express $G_{m,eq1}$ in terms of I_B. Then, for the flicker component of the PN, we use (28) where G_{m1} is substituted by the value of $G_{m,eq1}$ calculated earlier. After taking the derivative of the resulting equation with respect to I_B and equating to zero, we find

$$I_B = \left|\frac{N_6}{D_6}\right| \tag{75}$$

where

$$N_6 = 7V_{tank}n\left[(C_{1EQ}L_2 + C_2L_2 + C_{1EQ}L_2G_{m2}R_{DS2} + C_2L_2G_{m2}R_{DS2})s^2 + (C_{1EQ}R_{DS2} + C_2R_{DS2})s + 1\right] \tag{76}$$

DOI: 10.1002/cta

$$D_6 = \left(14C_{1EQ}L_2R_pn^2 - C_{1EQ}\Phi^2L_2R_pn^2 + 14C_{1EQ}L_2R_pG_{m2}n^2R_{DS2} - C_{1EQ}\Phi^2L_2R_pG_{m2}n^2R_{DS2}\right)s^2 + \left(14L_2 - \Phi^2L_2 + 14L_2G_{m2}R_{DS2} - \Phi^2L_2G_{m2}R_{DS2} + 14C_{1EQ}R_pn^2R_{DS2} - C_{1EQ}\Phi^2R_pn^2R_{DS2}\right)s - R_p\Phi^2n^2 - R_{DS2}\Phi^2 + 14R_pn^2 + 14R_{DS2} \quad (77)$$

The thermal noise contribution to PN does not exhibit a minimum. By examining (45), it can be observed that the PN due to the thermal noise decreases for higher values of I_B.

The total PN is given by (52) where the flicker and thermal components of the PN have been replaced by the new derivations. The total PN is plotted in Figure 11 versus the bias current density per unit of width I_B/W and validated by means of the results provided by SpectreRF simulations in Cadence, for a 1-MHz frequency offset from the carrier. In order to demonstrate the dependence of PN on L_2, the total PN is plotted for three different values of L_2. The maximum difference amounts to about 7 dB, observed for $L_2 = 1$ nH. The tank capacitance is such that f_0 is held at 10 GHz, whereas C_1 and C_2 have equal value. V_{B3} in Figure 2(a) is connected to V_{DD}, whereas V_{B4} has been swept from the value required to start up the oscillations to V_{DD}.

At 10 GHz, both theory and simulations predict a current density of about 0.075 mA/μm for which PN reaches a minimum. This value is independent of L_2 according to SpectreRF simulation results. However, from simulations, it appears that beyond the local minimum and a certain bias current density, further increases may offer a further slight reduction in PN for inductances of 2 and 3 nH. Thereby, in this case, it may be worth investing additional bias current in order to achieve improved PN performance.

From Figure 11, we can calculate the difference in PN between the values obtained for the bias current of 6.3 mA considered in Section 2, corresponding to a bias current density of 0.21 mA/μm, and the optimum bias current density of 0.075 mA/μm. SpectreRF simulation results for 10 GHz show a reduction of PN of about 3 dB for L_2 equal to 1 nH and optimum bias current density of 0.075 mA/μm.

By summing up the PN reduction provided by the inductive degeneration of 3 nH and optimum bias current density of 0.075 mA/μm, a potential overall reduction up to 14 dB can be achieved. Despite the current density of 0.075 mA/μm may lead to a better figure of merit, as mentioned earlier, it could be worth increasing the current consumption to 0.23 mA/μm in order to reach an overall potential reduction up to 16 dB.

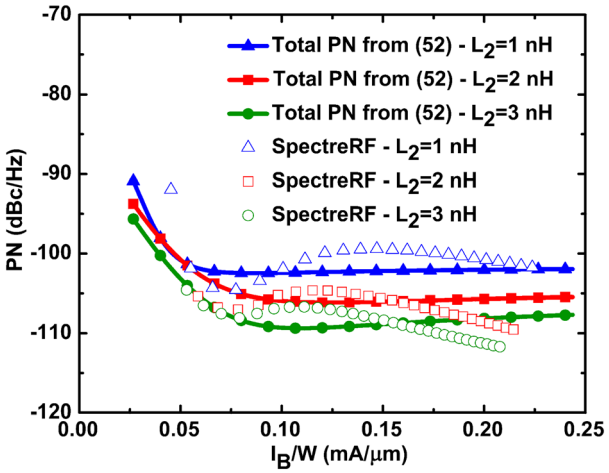

Figure 11. Total PN at a 1-MHz frequency offset from the carrier versus the bias current density I_B/W for the circuit of Figure 2(a), predicted by (52) and obtained by SpectreRF simulations for an oscillation frequency of 10 GHz.

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4.2. *Noise filter*

With reference to the Colpitts oscillator circuit topology of Figure 7(a), where a noise filter (L_3, C_3) has been introduced to the source node of M_1, for the PN component contributed by flicker noise, we use G_{m1} given by (74) into (70) in order to express $G_{m,eq2}$ in terms of I_B.

The value of G_{m1} in (28) is then substituted by the value of $G_{m,eq2}$ calculated before. After taking the derivative of the resulting equation with respect to the bias current I_B and equate to zero, we obtain the following expression:

$$I_B = \left|\frac{N_7}{D_7}\right| \tag{78}$$

where

$$N_7 = 7V_{tank}\left[L_3 n(C_{1EFF} + C_2)s^2 + n\right] \tag{79}$$

$$D_7 = \left(-C_{1EFF}L_3R_p\Phi^2n^2 + 14C_{1EFF}L_3R_pn^2\right)s^2 + \left(-L_3\Phi^2 + 14L_3\right)s - R_p\Phi^2n^2 + 14R_pn^2 \tag{80}$$

Again, the thermal noise contribution to PN does not exhibit a minimum. By examining (72), it can be observed that the PN due to the thermal noise decreases as I_B increases.

The total PN is given by (52) where the flicker and thermal PN components have been replaced by the new derivations. It is plotted in Figure 12 versus the bias current density I_B/W and validated by means of the results provided by SpectreRF simulations in Cadence, at a 1-MHz frequency offset from the carrier. In order to demonstrate the dependence of PN on L_3, the total PN is plotted for three values of L_3. The maximum difference is about 2 dB, observed for $L_2 = 3$ nH. C_1 and C_2 have equal size and are chosen to have f_0 equal to 10 GHz. C_3 is set equal to zero. V_{B5} has been swept from the value required to start up the oscillation to V_{DD}. Figure 12 shows that for $L_3 = 2$ nH, both theory and simulations predict a bias current density of around 0.375 mA/μm for which PN is minimized. Moreover, we can calculate the difference of PN between the results obtained for the bias current of 6.3 mA adopted in Section 3, corresponding to a current density of 0.21 mA/μm, and the optimum current density. From SpectreRF simulations, for instance, a PN reduction of about 6 dB can be achieved for L_3 of 2 nH and a current density of 0.36 mA/μm.

Overall, by summing up the PN reduction provided by the Colpitts topology with the noise filter for 3 nH and optimum bias current density of about 0.31 mA/μm, a potential overall reduction up to 19 dB

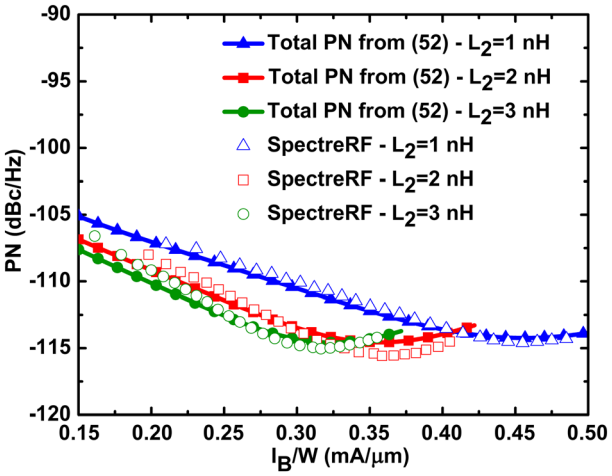

Figure 12. Total PN at a 1-MHz frequency offset from the carrier versus the bias current density I_B/W for the circuit of Figure 7(a), predicted by (52) and obtained by SpectreRF simulations for an oscillation frequency of 10 GHz.

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Table I. Summary of device sizing.

Transistor width (μm)		Capacitor value (fF)			Inductor value (nH)		
M_1	M_2	C_1	C_2	C_3	L_1	$L_{2,opt}$	$L_{3,opt}$
30	30	970	970	0	0.5	4	8

can be achieved with respect to −96.25 dBc/Hz of the traditional Colpitts topology [11]. Note that because of the very close PN performance, the case of 3 nH and 0.31 mA/μm lead to a lower current consumption and, thereby, potentially to a better figure of merit of the oscillator with respect to the case of 2 nH with a current density of 0.36 mA/μm.

5. CONCLUSIONS

The techniques of inductive degeneration and noise filter for the reduction of PN due to the tail transistor in CMOS LC oscillators have been applied for the first time to a single-ended Colpitts oscillator circuit topology. These techniques have been analyzed in detail by means of circuit theory and simulations. The analyses have allowed us to bring to the light a few interesting aspects not addressed yet in the literature.

In particular, an analytical expression of the oscillation frequency has been derived in order to allow an accurate prediction and show the dependence on the degeneration inductance and the noise filter components. In addition, an analytical expression of the PN has been derived in order to allow a good prediction and identify design opportunity for PN reduction in the previous techniques. The theoretical results, supported by circuit simulations, show that the PN of the Colpitts oscillator topology modified with the introduction of either the inductive degeneration or the noise filter reaches a minimum, leading to considerable potential benefits. In particular, there is an optimum degeneration inductance that resonates at the oscillation frequency with the parasitic capacitance at the source of the tail current transistor. In addition, for a given typical capacitance, there is an optimum inductance for which the noise filter resonates at the oscillation frequency. Last, it is possible to integrate a degeneration or noise filter inductor, in particular for an oscillation frequency of 10 GHz.

Moreover, a third technique for the PN reduction, namely, optimum current density, has been applied to the Colpitts topology with either the inductive degeneration or noise filter and analyzed in detail by means of circuit theory and simulations. It consists of biasing the oscillator circuit with the optimum current density for the minimum PN. The proposed analyses allow us for the first time to get an understanding of the theoretical details of this technique and its applications, identifying additional opportunities for the reduction of PN in the examined circuit topologies.

Overall, the analyses carried out for multiple degeneration inductances, noise filter inductances, and current density variations allow also some evaluations about the sensitivity of the respective PN reduction techniques.

The results of the analyses presented earlier show that, under the adopted common design conditions in a 28-nm CMOS technology, the previous techniques may potentially lead to PN reduction up to about 19 dB at a 1-MHz offset from an oscillation frequency of 10 GHz, with respect to the traditional Colpitts topology.

APPENDIX

The reference values of the circuit components used for the theoretical analyses and circuit simulations are reported in Table I. All the transistors have minimum length equal to 28 nm. In the adopted conditions, the transistors exhibit small-signal drain-to-source conductance g_{ds} of about 2.7 mS and gate resistance r_g of about 3 Ω.

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